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PILOT LINE III

GALLIUM ARSENIDE PILOT LINE FOR HIGH PERFORMANCE COMPONENTS

Contract No. F29601-87-C-0202

AT&T
Guilford Center

AT&T

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Semiannual Technical Report
for April through September, 1988

Prepared October 20, 1988

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GALLIUM ARSENIDE PILOT LINE FOR HIGH PERFORMANCE COMPONENTS

Semiannual Technical Report
October, 1988

1. INTRODUCTION (S. F. Nygren)

The Gallium Arsenide Pilot Line for High Performance Components (Pilot Line III) is to develop a facility for the fabrication of GaAs Logic and memory chips. The first eighteen months of this contract are now complete, and this report covers the period from March 28, 1988, through September 25, 1988. Also included with this report is an update of the Industry Survey of High Speed Packages.

During this reporting period, the construction of the User Friendly CAD System (HCAD) has continued its steady progress, and the cell array capability is being added. The PT-1 Logic and memory chips have proved invaluable, as our design, testing, materials, processing, and modeling personnel have used their data to explore the limits of the design and device targets and to specify the design targets for the next generation of devices. The first wafers from the first full-sized standard cell circuit, the Casino Test Chip, have been completed. Initial testing has shown some problems, and Failure Mode Analysis is being pursued aggressively. Total dose radiation tests on PT-1 HFETs, ring oscillators, and 256 bit SRAMs show less than 5% changes in electrical characteristic after exposure to $1x10^8$ rad (GaAs).

HCAD now includes HITS, a Hierarchical Integrated Test Simulator, and a re-implementation of N.2, an architectural simulator. The new macrocells have been inserted for use in standard cell circuit design, and HCAD is being used to design a Transversal Filter Chip, the second full-sized standard cell design done under this program. In addition, the Mentor Graphics toolset is being implemented for use in cell array designs.

Several circuits designed for this program are now in various stages of testing. The most interesting results are coming from the PT-1 memory, in which two logic families plus some linear circuitry must all function simultaneously, and the Casino Test Chip, which is our first experience with a 3500 gate, high-pin-count circuit. We have tested 7500 PT-1 memories, mostly by accepting all HFET wafers, regardless of their FET characteristics. We have found 15 devices with all 256 memory cells working at room temperature. However, many devices show exceedingly high power dissipation or contact failure (even when mechanical contact is confirmed). The first Casino Test Chips are on wafers having FET characteristics that are off-target. Some ring oscillators and straight-in/straight-out buffers are functioning, but all circuits show unexpected oscillations at their outputs. Failure Mode Analysis teams are now actively investigating these results, working to identify which features are related to the FET characteristics, which are related to circuit design, and which are related to wafer fabrication processes. In doing these analyses, the election beam prober is proving useful in probing internal modes in circuits.

Driven by the particularly stringent constraints of memory design, our design, testing, materials, processing and modeling personnel have examined the PT-1 results with a view toward identifying the best device targets for allowing designs with the highest possible noise margins. These targets have been selected, the MBE structure has been updated to meet them, and the next generation of devices is being designed: a PT-2M memory tester, a full custom ALU, a standard cell Transversal Filter Chip, and a 1000 gate cell array.

In the processing area, a cumulative total of more than 2000 MBE wafers have been grown for various purposes, and the present capacity is 48-56 wafers/week. A third MBE machine has just been moved into place. Almost 300 of these wafers have completed processing as PT-1, PT-2L, or Casino Test Chips. And directed attention has caused the processing interval to drop from 100 working days last December to 45 working days in September, 1988. Official documentation for the baseline technology is in place, and processing is now under change control. The AlGaAs removal etch has been automated and is now more reproducible, and the gate length has been made more reproducible by improving control of photoresist thickness. There remains a problem with an annealing procedure where material transport from one wafer to another is depositing GaAs particles on wafer surfaces.

Development of the advanced technology is proceeding, with a goal of demonstrating 400 MHz performance next summer. In addition to the short gate SQT transistors and the reduced design rules, the advanced technology will use an improved version of the SFFL Logic family and a lower dielectric constant intermetal insulator.

Total dose radiation experiments have been carried out up to a dose of 6×10^8 rad (GaAs). After 1×10^8 rad (GaAs), HFETs, ring oscillators, and 256-bit SRAMs all showed less than 5% change in electrical characteristics. Ring oscillators and inverters recover promptly after radiation pulses at dose rates less than 1×10^{10} rad (GaAs)/sec. The SRAMs available for test had low noise margins; but when marginal cells were masked, a threshold of 1×10^9 to 2×10^{10} rad (GaAs)/sec was observed in two devices. Single event upset measurements showed error rates of 5×10^{-8} errors/bit day for rad hard cells, and 2×10^{-7} errors/bit day for standard cells. New electron migration experiments on the Ti/Pt/Au metal system predict a 10^8 hour median time to failure at 10^5 A/cm^2 and 55°C.

2. DESIGN

2.1 HCAD: A User Friendly CAD System (L. R. Fisher)

The third six months of the Pilot Line III program saw substantial advances made in the development of the User Friendly CAD System, now called HCAD. In light of the progress made, the second GaAs chip to be designed at Hughes, the Transversal Filter Chip, is being designed with HCAD.

HITS, the Hierarchical Integrated Test Simulator from the Naval Air Engineering Center, was integrated into HCAD and is now a functional part of the system. Simulation models have been developed for the elements of the AT&T Pilot Line III standard cell library to support the use of HITS for Automatic Test Pattern Generation.

The integration of N.2, the architectural simulator from Zycad (formerly from Endot), was re-implemented to provide increased performance and flexibility. The improved integration features new menus, better support for hierarchy in the N.2 topology file, and closer coupling with the Simulation Interface within the SDA Framework. Note that SDA is now called Cadence, following a merger with ECAD. In addition to better integrating the N.2 tools, higher level N.2 models for the AT&T Pilot Line III standard cell library have been developed. These models result in significant performance improvements, with compile and simulation times being reduced by 20 to 60 percent.

Several gate array or configurable cell array layout tools were evaluated for compatibility with the AT&T floorplan and cell personalizations. Included in the evaluation was the gate array toolset sold by Mentor Graphics. This toolset includes support for fully automatic placement and routing as well as support for interactive, semi-automatic placement and routing with a design-rule correct graphics editor. The Mentor toolset was selected to implement support within HCAD for gate array layout, and integration of the toolset is now in progress.

AT&T has developed a new standard cell library consisting of more complex functions than exist in the initial cell library. These new cells are called macrofunctions. The new macrofunctions have been inserted into HCAD and are being used in the design of the Transversal Filter Chip. Addition of these macrofunctions resulted in the addition of over 100 new gate level and circuit level schematics, as well as the layouts (provided by AT&T) and layout abstracts (used by the standard cell place and route tools). The following table lists the new macrofunctions now supported in HCAD.

The technology files in HCAD have been updated as necessary to track new developments and changes in the Pilot Line III technology. The layout design rule technology file, for example, was updated to conform to the design rules released in the Design Manual.

Cell Name	Function	layout	symbol	gate.sch	gaas.sch
aoi3333	and-or-invert	yes	yes	yes	yes
barsrb4	barrel shifter	yes	yes	yes	yes
bclab4	adder	yes	yes	yes	yes
bme	multiplier/encoder	yes	yes	yes	yes
bmfab4	booth multiplier	yes	yes	yes	yes
bmhab4	booth multiplier	yes	yes	yes	yes
bmmuxb4	booth multiplier	yes	yes	yes	yes
ckdrv_m	clock driver	yes	yes	yes	yes
clab4	adder	yes	yes	yes	yes
clcb4	carry lookahead	yes	yes	yes	yes
ctrdb4	down counter	yes	yes	yes	
ctrdpb4	down counter	yes	yes	yes	
ctrub4	up counter	yes	yes	yes	
ctrudb4	up/down counter	yes	yes	yes	
ctrudpb4	up/down counter	yes	yes	yes	
ctrupb4	up counter	yes	yes	yes	
daoi22	dual and-or-invert	yes	yes	yes	yes
daoi32	dual and-or-invert	yes	yes	yes	yes
daoi33	dual and-or-invert	yes	yes	yes	yes
decb4	decoder	yes	yes	yes	yes
dinrb	dual inverter	yes	yes	yes	yes
dmux	dual multiplexor	yes	yes	yes	yes
dnr2	dual nor	yes	yes	yes	yes
dnr3	dual nor	yes	yes	yes	yes
dnr4	dual nor	yes	yes	yes	yes
dnr5	dual nor	yes	yes	yes	yes
dxnor	dual exclusive nor	yes	yes	yes	yes
dxor	dual exclusive nor	yes	yes	yes	yes
fadd	adder	yes	yes	yes	yes
fd1s2ax_m	flip-flop	yes	yes	yes	yes
fd1s2dx_m	flip-flop	yes	yes	yes	yes
fd1s2nx_m	flip-flop	yes	yes	yes	yes
fd1s5f_m	flip-flop	yes	yes	yes	yes
hadd	adder	yes	yes	yes	yes
regfb44	register file		yes	yes	yes
scanrfb4	register file	yes	yes	yes	yes
sdatemplate	unspecified	yes	yes	yes	yes
sigdrv_m	driver	yes	yes	yes	yes
srmxpib4	shift register		yes	yes	yes
srpipob4	shift register		yes	yes	yes
srpisob4	shift register	yes	yes	yes	yes
srrfb4	shift register	yes	yes	yes	yes
srsipob4	shift register	yes	yes	yes	yes
tbfin_m	tri-state buffer	yes	yes	yes	yes

Summary of HCAD Macrofunction Library

2.2 DEMONSTRATION VEHICLES

2.2.1 PT-1 Test Results (AT&T Memory) (W. R. Ortner)

Binning Results

A total of 150 PT-1 wafers were tested thru September, 1988. The binning results are summarized in the following table.

Bin	Description	Rad Hard		Standard		Total	
31	Shorts	910	24.27%	767	20.45%	1677	22.36%
30	Contact Failure	380	10.13%	414	11.04%	794	10.59%
29	Non Functional Hi Power	1050	28.00%	1114	29.71%	2164	28.85%
28	Non Functional	1400	37.33%	1450	38.67%	2850	38.00%
10	Functional Hi Power	1	0.03%	0	0.00%	1	0.01%
2	Functional	9	0.24%	5	0.13%	14	0.19%
1	Good	0	0.00%	0	0.00%	0	0.00%
		3750		3750		7500	

Shorts Failures are devices in which at least one power or signal lead draws more than 10ma at 100mv with all other leads at ground. Contact Failures are devices where at least one power or signal lead fails to conduct at least 50microamps, even though mechanical contact has clearly been made between the probes and the chip. Functional devices have 256 independent working memory cells capable of storing both a one and zero logic state. Non-Functioning devices fail to meet the above criterion. Devices failing the maximum IDD (108ma) or IDDA (36ma) are binned as HI Power. A Good device passes all specified tests. We are now pursuing an aggressive Failure Mode Analysis program to determine the causes for the large numbers of shorts, high powers, and contact failures.

Distribution of Working Bits

A comparison of working cells for Rad Hard vs Standard designs, at 50MHz and 200MHz, is shown in Figure 1. The first point contains the number of devices which had from 0 to 9 working cells and the last point contains the number of devices which had from 250 to 256 working cells. Intermediate points are 10 to 19 ... etc. The number of working cells seems randomly distributed, with a slight increase at 220-256, and large number at zero. We believe that this is not due to processing failures. Rather, the problem is that the actual FET characteristics are not sufficiently close to the design targets. As a result, the devices do not function properly. The Failure Mode Analysis effort is investigating this in detail. On the bright side, the standard and rad hard designs have equivalent performance, so we expect the rad hard design will enhance radiation hardness without sacrificing manufacturing yield.

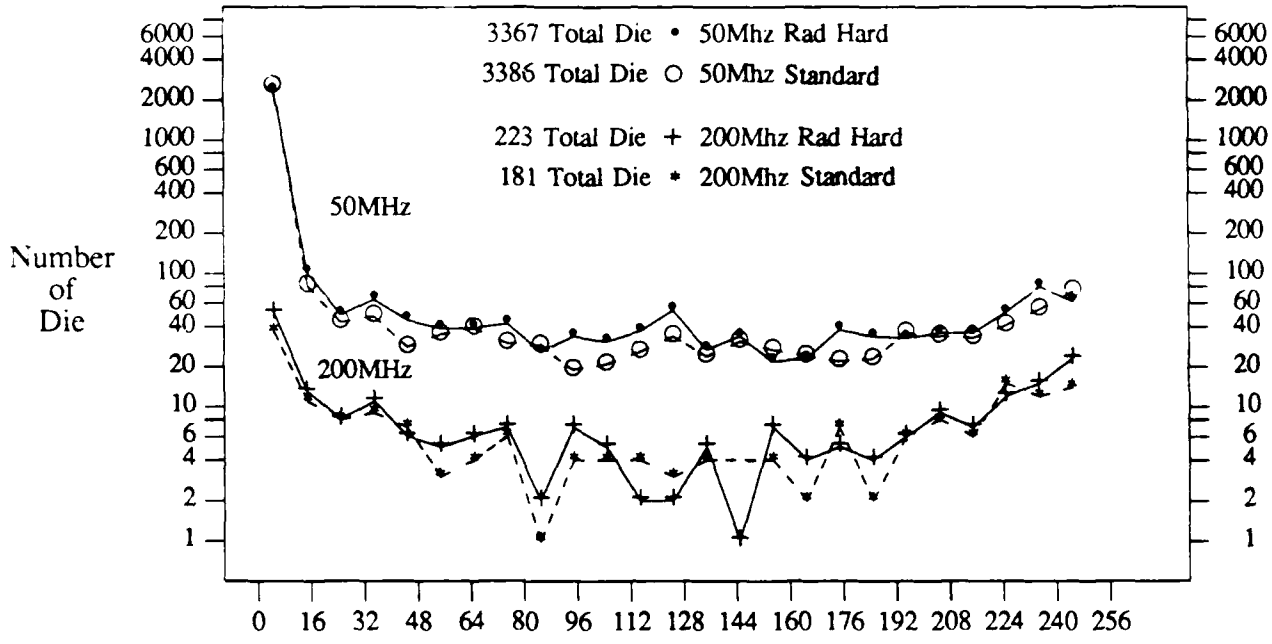


Figure 1. Number of Working Cells in PT-1 Memories.

2.2.2 Laser Programming (R. T. Smith)

The main objectives during this reporting period were to refine the processing window for laser programming using PT-1 wafers, and to freeze the laser/test strategy and develop the initial software for PT-2 repair. Unfortunately, due to unforeseen delays in PT-2M schedules, completion of the latter objective awaits arrival of PT-2M wafers.

In the meantime, good progress has been made in refining the laser programming process window using PT-1 wafers with so-called laser windowed passivation. In the previous semi-annual report, this structure was described together with a curious target-link orientation dependence. Specifically, links oriented horizontally (parallel to the front face of the laser system) could be exploded at a lower threshold energy than vertically oriented links, and with a wider energy window. At the time, the main candidates to explain this dependence on link orientation were laser polarization or astigmatism in the final objective lens of the beam positioning system. Both of these possibilities have been eliminated from further consideration by careful experimentation. The most likely culprit at this stage appears to be asymmetry in the spatial profile of the focussed laser spot. Work is continuing with a view to exploiting what at first glance appeared to be a drawback. The good news is that the process window for horizontal links is both wider and cleaner than that obtained with a circularly symmetric spot, while the window for vertical links is substantially equivalent to the symmetric case.

Hardware development has been completed to prepare the automated parametric tester for evaluation of laser test structures on PT-2M. The strategy for off-line test and analysis of PT-2M 256 bit memories has been refined and transfer of files from the Teradyne J937 memory test system to a VAX 11/750 host computer demonstrated. File transfer of laser coordinates from the VAX 11/750 to both Teradyne M118M and ESI 8000C laser systems has also been debugged. Further work awaits the imminent submission of PT-2M to the mask shop and subsequent wafer processing.

2.2.3 PT-1 Test Results (AT&T and Hughes Logic) (L. Ackner, W. B. Leung)

In the last semiannual report, the test results of logic circuits in the first few PT-1 wafers were reported. All logic circuits were found to be functional, with propagation delay slightly higher than simulation results. Over the last six months much more data on wafer yields, wafer probing results, and package measurements were accumulated. These data are given in the following two tables.

A total of 119 wafers were tested. A steady improvements in wafer yield was observed as more experience was gained in processing. In recent lots wafer lot yield of 10 sites (45.5%) was recorded for the 6x6 multiplier which has 3072 transistors. And wafer lot yield of 19.5 sites (88.6%) was recorded for the 8 bit comparator which has 412 transistors. Some of the functional chips were packaged in the TriQuint 44 pin package and delivered to DARPA. The performance of the packaged circuits is better than the wafer probing results because of a better testing environment. From these test results, the propagation delay through a gate is found to be 100 - 200 ps, which is faster than necessary to meet the minimial contract goals.

Besides the regular testing of wafers and packages, experiments on high speed testing were conducted. The 4 bit adder circuit has been tested successfully at 200 Mbps. Testing of packages over the high temperature region has also been done. Preliminary results indicated that the 4 bit adder circuit is fully functionally over the temperature range of 25 - 150°C.

The PT-1 logic circuits have accomplished their goals as test chips for design methodology and CAD tools.

Wafer Lot	No. of Wafers	Multi-plier	Adder	Delay Chain	Multi-plexer	Comp-arator	Shift Register	Counter
11210	1	4.00	6.00	NA	9.00	6.00	6.00	1.00
30040	5	2.00	5.20	NA	9.80	7.40	2.20	2.20
30050	5	0.60	2.60	NA	6.60	2.00	1.20	0.80
30060	3	2.70	8.00	NA	10.00	8.00	6.00	6.00
30070	4	0	6.00	NA	8.00	4.25	0.25	1.25
30080	4	2.00	6.25	NA	13.25	5.30	1.50	1.00
30090	3	0.67	5.00	NA	8.67	4.33	0.33	0.33
30100	2	1.00	6.00	NA	14.00	13.50	6.00	1.50
30110	4	0.00	4.25	NA	4.50	4.25	2.25	0.50
30120	8	1.00	3.25	NA	7.88	6.00	2.75	2.13
30130	6	6.50	13.00	13.50	12.83	12.00	12.00	9.17
30140	3	4.33	12.00	4.00	16.33	14.67	10.00	9.33
30150	8	2.38	3.75	2.38	8.25	13.38	4.00	2.38
30160	7	6.00	7.71	5.14	7.43	12.70	6.00	5.43
30170	5	5.80	11.00	NA	11.60	11.80	9.80	10.20
30180	4	4.00	7.75	4.25	9.50	11.75	8.25	2.50
30190	2	7.50	9.50	4.00	11.00	13.50	11.50	9.00
20210	3	0.33	6.00	3.33	5.33	11.00	3.00	2.67
30220	1	5.00	10.00	11.00	13.00	16.00	6.00	11.00
30230	5	4.40	7.40	NA	17.00	11.00	6.40	5.00
30240	8	3.38	6.38	4.88	7.75	9.00	4.25	4.38
30250	8	4.13	7.75	13.88	11.25	7.75	6.63	9.13
30260	8	7.63	12.38	12.00	14.13	16.25	9.13	8.38
30270	7	0.71	3.14	0.29	6.14	11.57	0	0
30280	2	10.00	12.50	11.50	17.50	19.50	15.50	12.50
30330	3	1.67	7.00	7.67	7.67	11.00	2.67	1.00

Functional test was done at VDD = 2V, T = 25°C, at 1 MHz.
There are 22 test sites per wafer.
NA = data not available.

PT-1 Wafer Lot Yield Summary

Each value is the average number of good devices on a wafer from the indicated lot.

Circuit	Wafer #	# of Pkgs	Average Prop. Delay (ns)	Average Dynamic Current (mA @ 1 MHz)	Average Minimum VDD (V)
6 Bit Multiplier	11212	2	5.81	224.8	1.80
	30047	5	5.00	306.5	1.95
	30048	2	4.69	328.4	1.79
	30063	1	5.88	264.0	1.87
	30176	5	6.01	299.2	
	30177	7	6.41	284.0	
	30233	9	4.653	342.5	2.02
4 Bit Adder	30045	1	4.75	133.4	1.60
	30047	4	3.95	185.4	1.26
	30048	5	5.00	192.4	1.69
	30176	10	3.30	177.6	1.45
	30177	6	3.35	177.4	1.45
16 Bit Multiplexer	30047	2	2.68	76.7	1.33
	30048	6	2.54	84.8	1.26
	30057	8	3.97	63.1	1.37
	30063	1	3.125	409.6	0.96
	30176	5	3.65	72.0	1.34
	30177	9	3.85	62.5	1.38
	30233	6	2.65	89.6	1.36

PT-1 Package Test Results.

2.2.4 Casino Test Chip Test Effort (E. K. Gee and W. T. Kuo)

In the period from April through September, 1988, test equipment was prepared for examining the Casino Test Chip (CTC). By the end of this reporting period, initial testing of the CTC had been performed on three wafers. Functional circuits were found in a 15-stage ring oscillator and a Straight-In/Straight-out buffer circuit.

One of the high risk technical issues is the manufacturability of the 241-pin probe card for the CTC. Micro-Probe Inc. of San Diego was not only able to deliver the probe card in time but with excellent quality. Probe placement was very accurate despite the high pin count and tight pad spacing of the CTC. (0.004 in. pads on 0.005 in. centers) Test software development and final fixture debugging were completed after receiving the CTC probe card and first lot of wafers.

Four wafers containing the Casino Test Chips were parametrically tested by AT&T and then delivered to Hughes for functional testing at the end of August. Initial parametric data show relatively higher threshold voltages and lower transconductance than the design targets. Functional test data demonstrated some working circuits after probing three wafers. Average power consumption of the CTC was measured to be 3.3 Watts.

Various sections of the CTC were tested individually for functionality. The 15 stage (buffered inverter) Ring Oscillator was measured with a high bandwidth oscilloscope to observe its waveform. The average frequency of oscillation was found to be 200 MHz for two wafers.

The yield on the Ring Oscillator structure was 21/37 on one wafer and 8/37 on the other, as shown by the wafer maps of Figure 2. The rise and fall times of the Ring Oscillator were measured to be about 700ps at the probe card level, as shown in Figure 3.

A second structure, a Straight-In/Straight-Out buffer, was also tested. This structure contained one input receiver that fanned out into four output drivers. During initial testing, all of these circuits oscillated. Many experiments were performed to locate the source of oscillation. Various loads were used on the outputs of the CTC as well as extra decoupling capacitors for the power supplies to reduce the amplitude of oscillation. There were two conditions that would help reduce the amplitude of oscillation:

1. When the output pins were open circuited one at a time. The more pins that were open circuited, the smaller the amplitude of oscillation.
2. When current loads were connected at the outputs. The smaller the current loads, the smaller the amplitude of oscillation.

There was strong evidence that the oscillation was caused by high transient load currents and the fact that the input receivers and the output drivers shared a common VDD power bus at the chip level. Noise could be coupled back to the input receivers via the VDD bus due to the fast edge rates of the GaAs circuit outputs. To confirm this, a YAG laser was used to separate the VDD power bus between the input receivers and output drivers on the wafer. The oscillation was either smaller in amplitude or no longer present after lasering.

Further testing of the other sections of the CTC such as the 8x8 Matrix Switch, MUX/DMUX circuit, and the Boundary Scan will be explored after lasering the VDD power busses of the rest of the wafers.

2.2.5 IDS-5000 E-beam Probing Results (E.K. Poon)

The PT-1 input buffer consists of two inverters. The first one is of the non-buffered type and the second one is buffered for high drive. In the measurement, input signal B1 of the 4-bit adder was toggled at various frequencies and the signals at different nodes inside the buffer were measured using the IDS-5000 E-beam system. In the measurements, the same time scale and voltage scale were used throughout.

The results, which are shown in Figures 4 to 9, are summarized below. Except for Figure 9, the input signal B1 had a 2 ns rising edge. In Figure 9, the transition time is only 1 ns. Input signal swing is from 0.2 V to 1.5 V. Although the scale shown in the figures is 500 mV/div, it cannot be taken literally because the IDS-5000 system only gives relative voltage measurement.

1. At low frequency (Figures 4, 6 and 7), there is a substantial delay across the buffer for the rising edge of the input signal. This behavior was observed in various chips on various wafers. The delay is due to the poor pull-down of the INRG gate in the input buffer. The result is a loss in signal width, as can be seen clearly in Figure 7. This result may explain the discrepancy between the simulation results and the measured propagation delays for PT-1 devices. The falling edge, however, behaves much better as can be seen in Figures 5, 7, 8, and 9.

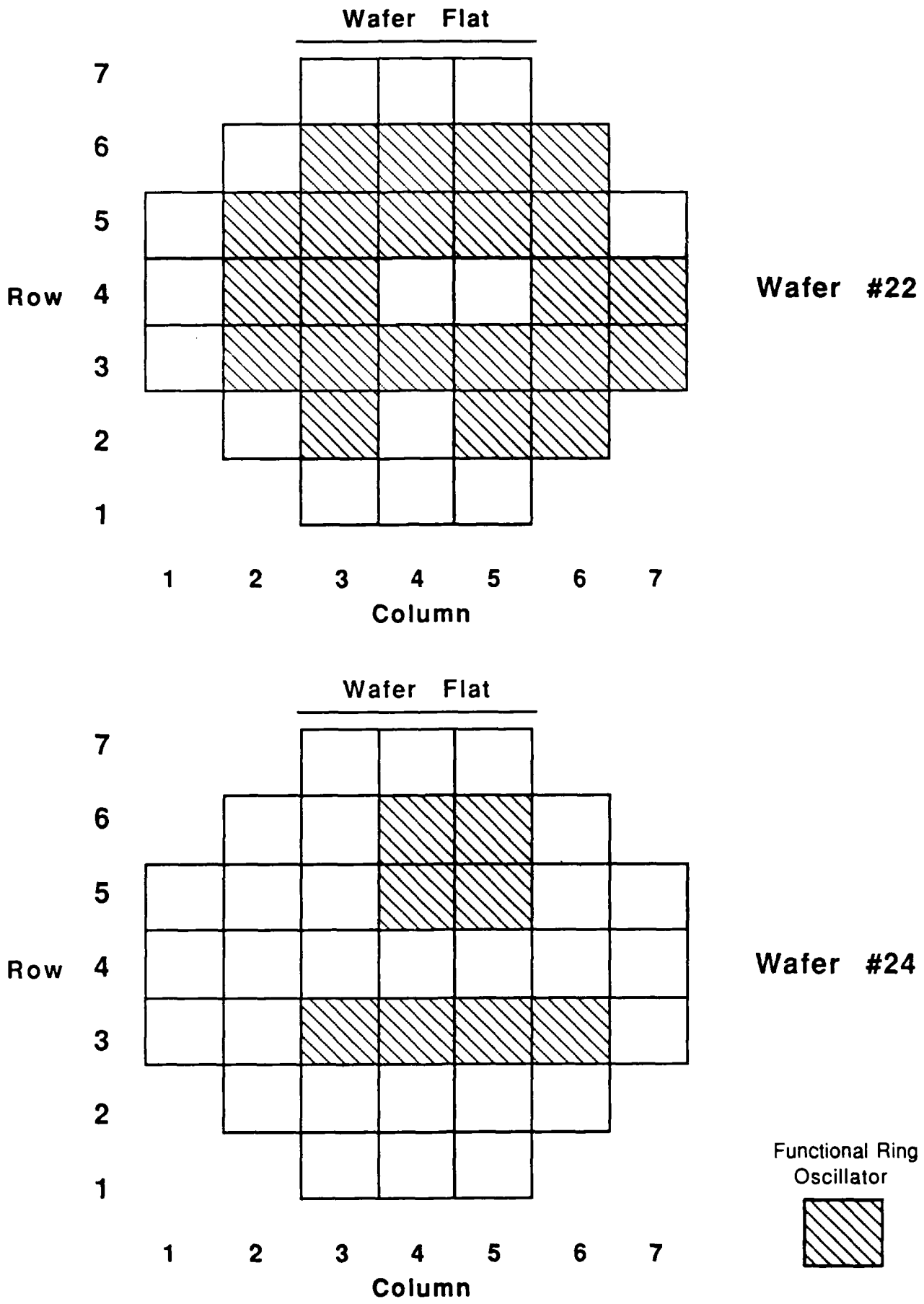
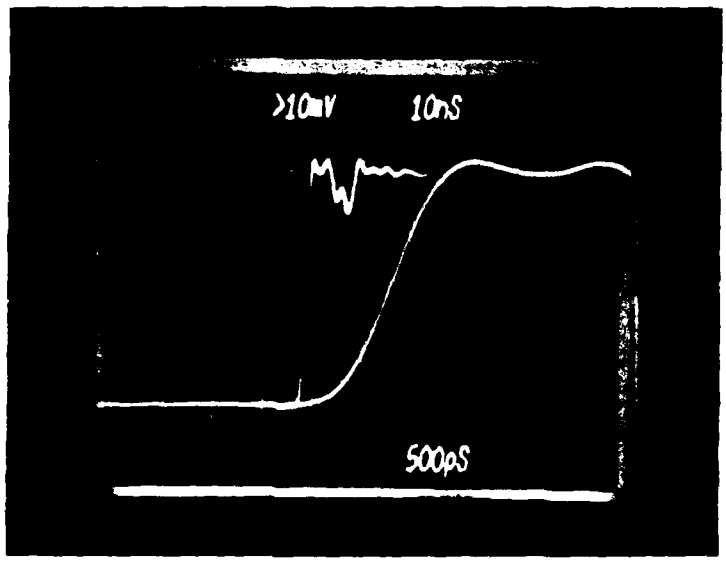
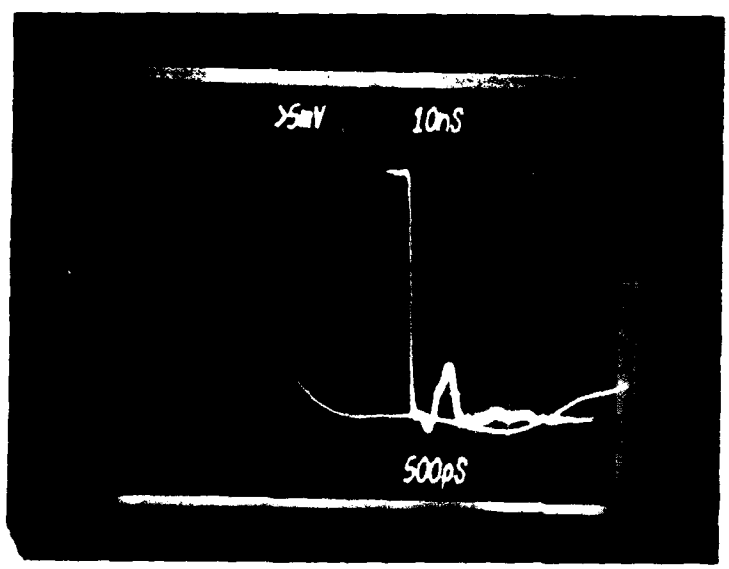


Figure 2. Maps Locating the Good Ring Oscillators in Two Casino Test Chip Wafers.

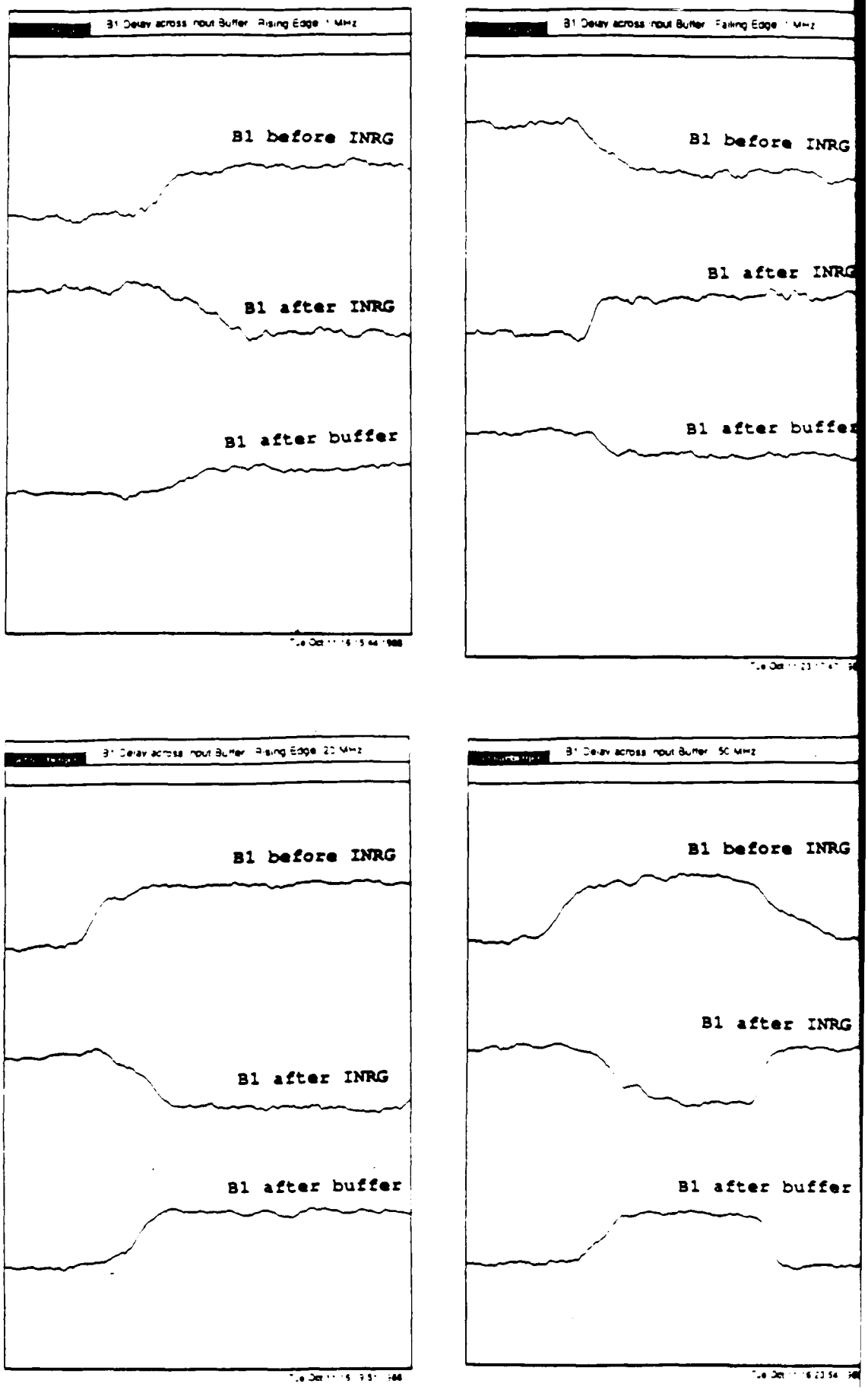


Rise Time

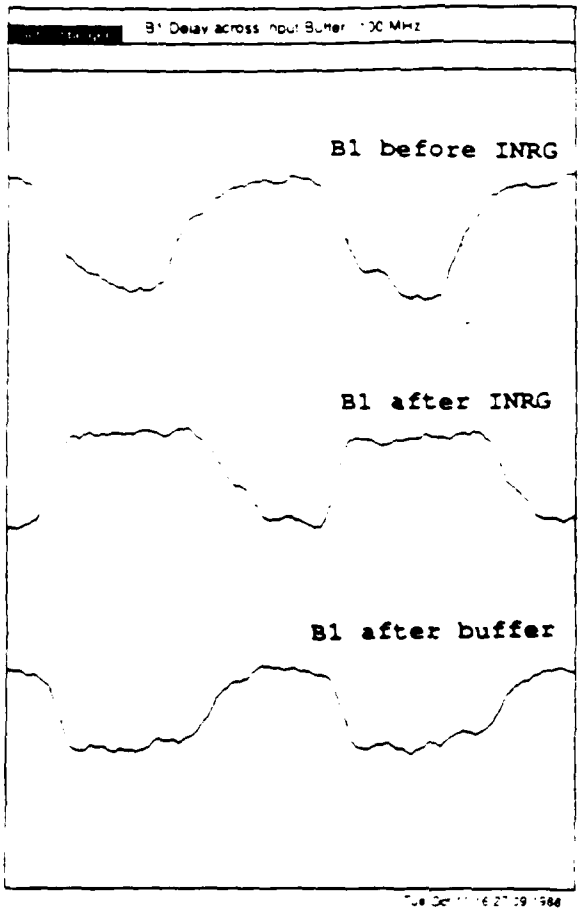


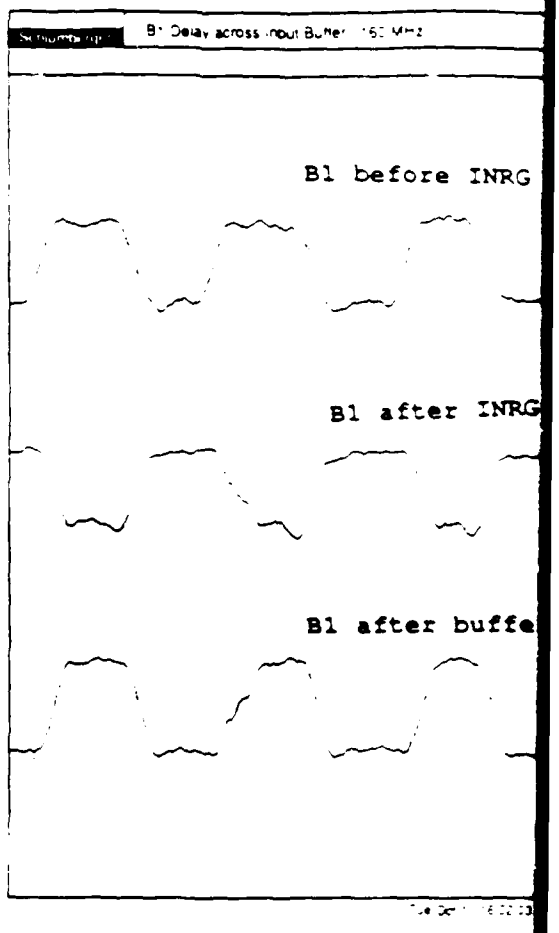
Fall Time

Figure 3. Oscilloscope Pictures Showing Rise and Fall Times of the CTC Ring Oscillator.



Figures 4-7. Data from the Electron Beam Prober Showing Delay Times within the PT-1 Input Buffer. See the text for details.





Figures 8-9. Data from the Electron Beam Prober Showing Delay Times within the PT-1 Input Buffer. See the text for details.

2. At high frequency, the propagation delay of the rising edge across the input buffer decreases. The transition time of the edges (1 ns in Figure 9), may also play an important role in the operation of the logic gates.

2.2.6 PT-2M Design (DePaolis)

The process tester PT-2M memory is a 256 bit clocked SRAM with many of the features that will be incorporated on the 4K SRAM design. A block diagram of PT-2M is shown in Figure 10. Design work continued on PT-2M up to the point where the design was ready for the mask shop in early June. At that time several events caused the design to be put on hold. Measured PT-1 memory circuit performance results did not agree with simulated values. In particular, input buffer minimum high levels (Vih-min) were being measured 300 mV greater than what was being simulated. The Vih-min levels were first measured on the Teradyne and then confirmed on a manual bench set. Figure 11 shows the distribution of Vih-min as measured on PT-1 wafers and a basic PT-1 input buffer. With an input voltage range specification of 0.2 V to 0.8 V, there was no margin for this magnitude of error. Serious doubt was then cast on the ability to accurately simulate the SFFL, DCFL, and linear circuits used on PT-2M. A second event that caused an alarm was process control data showing that the FET characteristics were not on target. Measurements made at Reading on other PT-1 circuits confirmed our findings and work was begun to solve the problem.

The results of many investigations and experiments resulted in the issuance of new model files (sargicS.11). The new models address the issue of process variations with high, nominal, and low current FET models at 25°C and 125°C. The process technologists negotiated the threshold voltages and E/D device ratios with the memory and logic designers. It is with these new model files that PT-2M circuits are now being optimized for maximum noise margins and functionality. The new projected mask shop date is October 14, 1988. We believe the extra effort to close the simulation-device test loop is the best assurance for the success of the 4K SRAM design. All of the PT-2M circuits will be used on the 4K design. A 4K array model will be simulated shortly after PT-2M is in the mask shop and work will begin on circuit optimization.

More recent testing of the PT-1 memory on the IDS-5000 e-beam prober revealed a problem with the row select-deselect timing. According to simulations performed prior to PT-1's mask shop date, a new row of cells was only selected after the previously accessed row was deselected. Actual e-beam probe measurements show multiple rows being selected causing potential cell to cell interaction and upset of data. This is further proof that the device models were not giving us actual device size ratios that emulated real circuit performance.

2.2.7 PT-2L Design (W. B. Leung, Y. K. Lo, W. A. Oswald, E. K. Poon)

The process tester PT-2L is implemented as a test vehicle for fairly large logic circuits with over 2k gate complexity. Four circuits were included in PT-2L. The design methodology and the function of these circuits were discussed in the last semiannual report. A diagram of the custom design methodology for Memory Tester is shown in Figure 12. The summary of basic

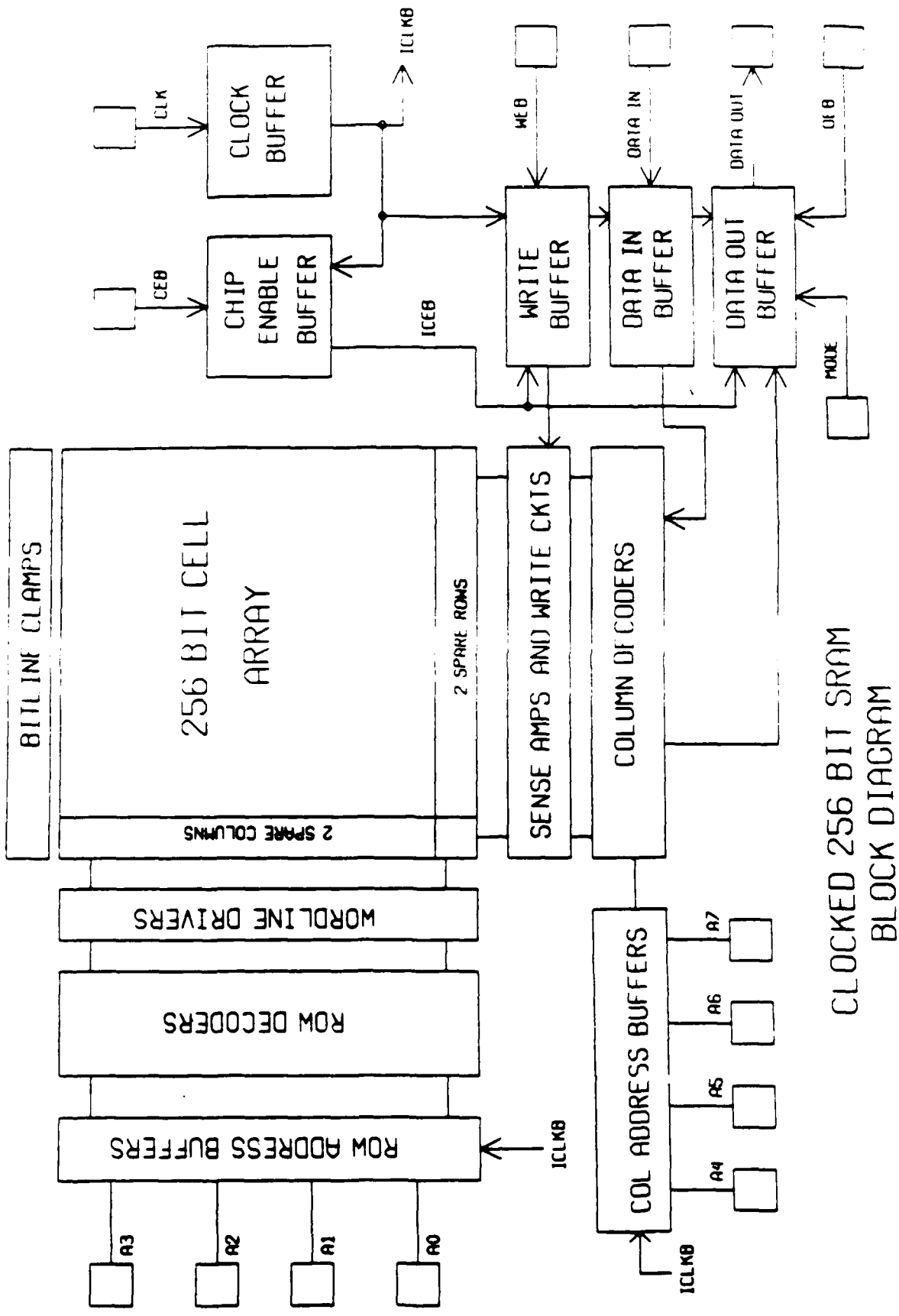
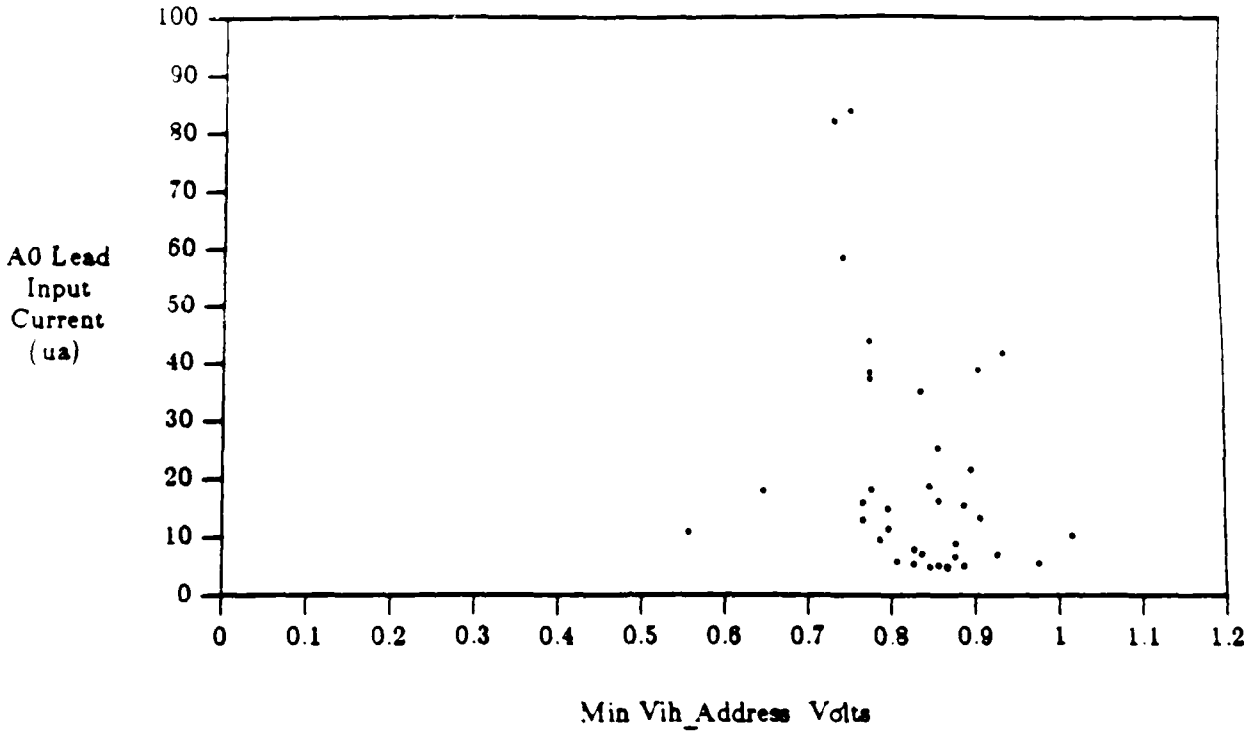


Figure 10. Block Diagram of the PT-2M Memory.

Vih-min and Input Current Characterizations



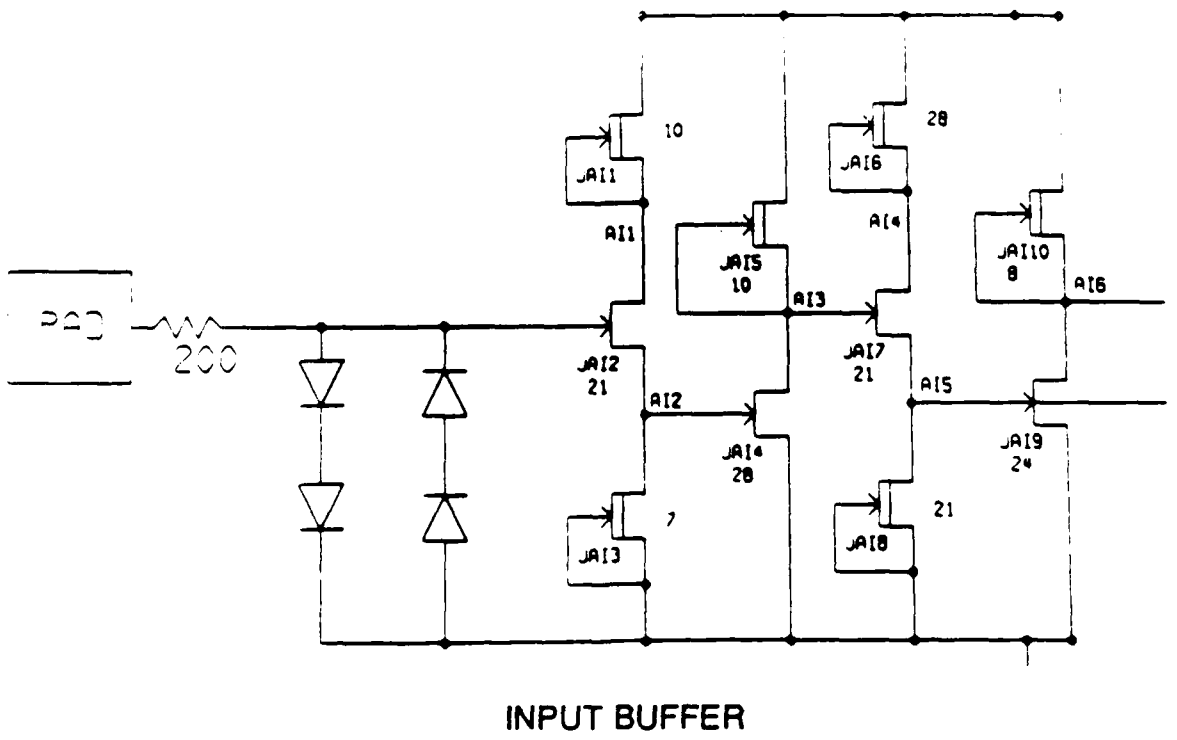


Figure 11. The PT-1 Memory Input Buffer Schematic and its Vih-min Levels.

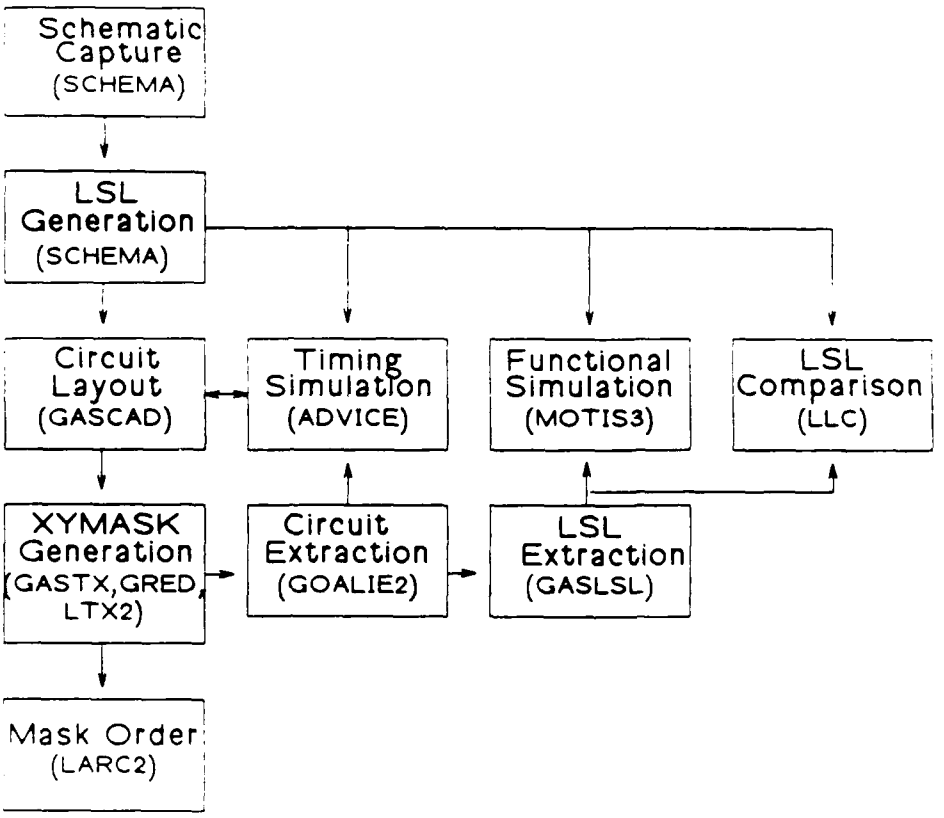


Figure 12. PT-2L Memory Tester Design Methodology.

information for these circuits is presented below. Figure 13 shows the circuit layouts.

Circuit	Logic Design	FET Count	Gate Count	I/O
ALU DEMO I	MDAC	15147	2211	60
Dual 8 x 8 Multiplier	ALC	11850	1778	66
Quad 4-Bit Adder	ALC	3192	364	56
Memory Tester	Mayo	11993	1723	61

*MDAC = McDonnell Douglas, ALC = AT&T Bell Laboratory at Allentown-Cedar Crest.

PT-2 Logic Test Circuits

The design of all four circuits were completed and verified in April. However the I/O buffers had to be modified due to a change in specification. The mask set for PT-2L was ordered in June. Test vectors, test programs, probe cards, and test fixtures are all in place for the testing of PT-2L circuits when they are available.

2.2.8 BSTS Transversal Filter Chip Design (S. W. White)

Deliverable Circuit E has been chosen to perform a Transversal Filter function found in the BSTS Signal Processor. This design utilizes the speed advantages of a pipelined architecture and the superior mobility of Gallium Arsenide to perform serially with a single processor the operations performed by many Silicon CMOS Transversal Filter processors (chips) operating in parallel. The actual function performed by the chip is that of a non-recursive digital filter based on a discrete implementation of convolution. Time samples of infrared detector data are correlated with the expected impulse response of a target profile to increase the incoming data's signal-to-noise ratio.

The architecture for the chip was chosen to achieve a 200 MHZ clock rate while utilizing approximately 5000 equivalent gates. This architecture includes a multiply/accumulate function for processing the convolution integral, a Register File for storing the tap weight coefficients associated with the expected impulse response, and an external memory interface and controller. A high-level block diagram of this architecture is shown in Figure 14.

A chip specification detailing functional, electrical, and timing characteristics has been developed based on information obtained from BSTS Systems Engineers. Following this development, a complete logic design utilizing the existing standard-cell library was generated, with particular attention paid to the design of high-speed multiplication and addition units. In addition to this standard cell version, a "macrofunction" implementation has been pursued after an initial investigation revealed that such a design could be advantageous with respect to chip size, clock rate, and power dissipation. To this end, macrofunctions were specified for development which were both general purpose in nature, and suited for the Transversal Filter

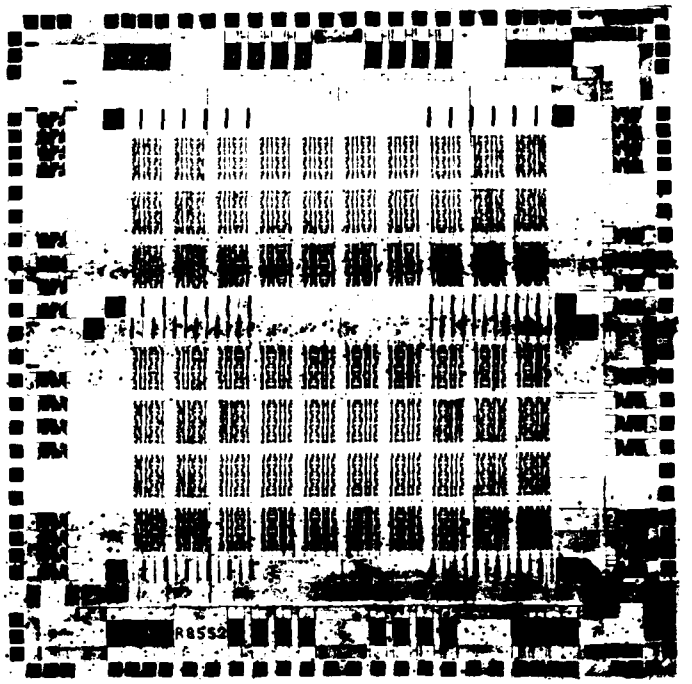


Figure 13a. PT-2L Quad 4-Bit Adder Layout.

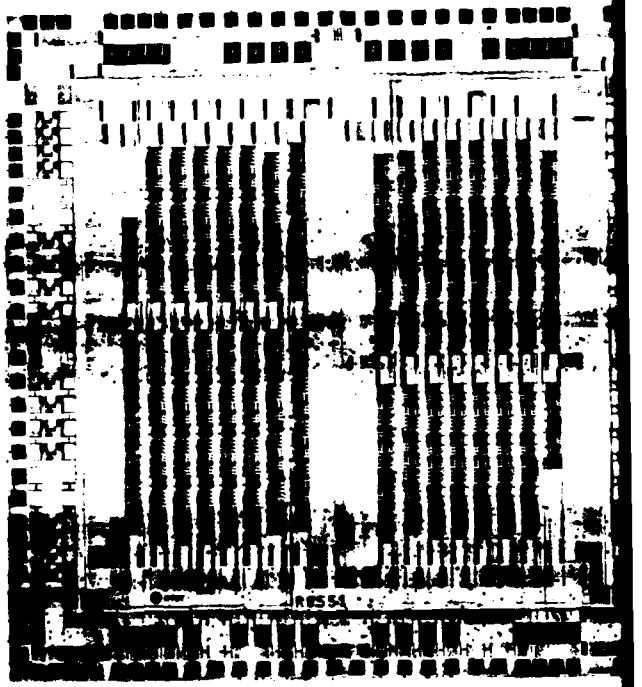


Figure 13b. PT-2L Dual 8 x 8 Multiplier Lay

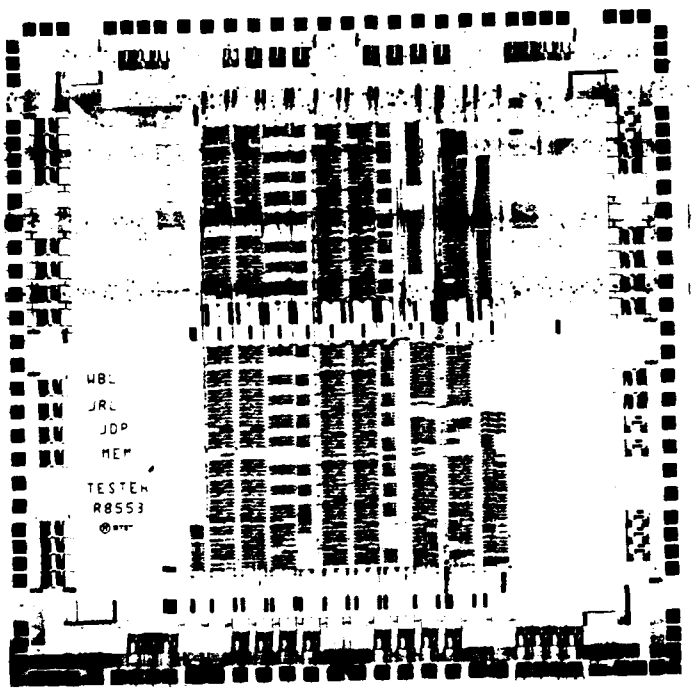


Figure 13c. PT-2L Memory Tester Layout.

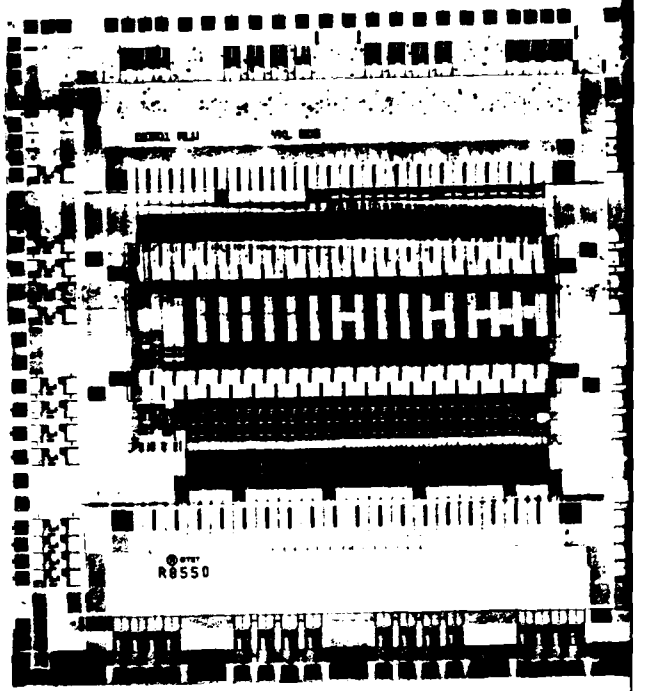


Figure 13d. PT-2L ALU DEMO I Layout.

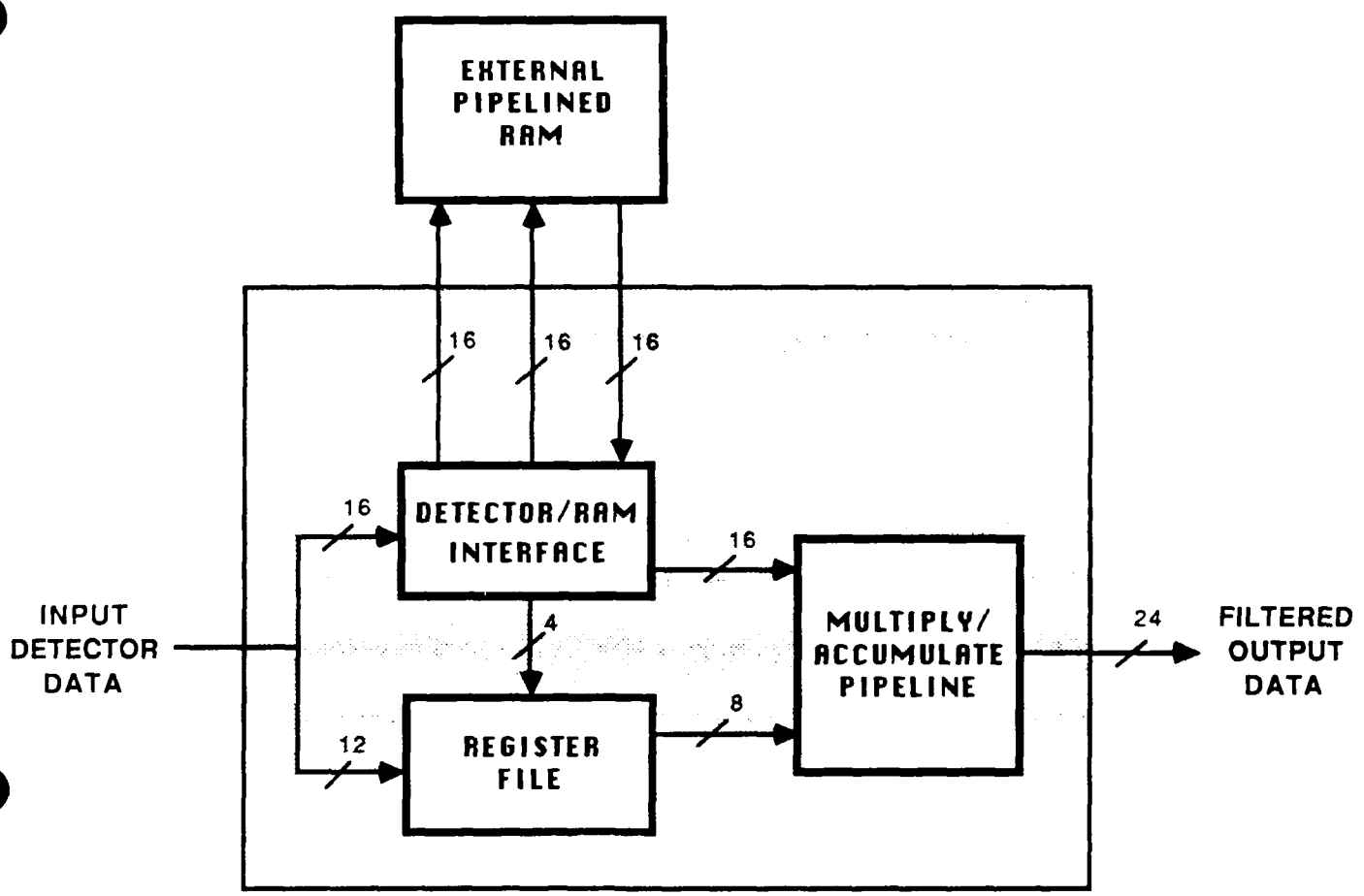


Figure 14. Transversal Filter Chip Architecture.

design. Subsequently, a logic redesign was performed which resulted in a macrofunction implementation of the chip. Further work on this design awaits completion of the new macrofunction library.

The standard-cell logic design was captured using the MENTOR schematic capture tools. These schematics were then translated using a Hughes-developed tool to generate schematics within the HCAD system. This translation proved to be much more time consuming than expected due to limitations in the translation program itself. Once the schematics existed within HCAD, the remaining HCAD tools could be run including a statistics program which indicated that this standard-cell design contains approximately 5.5K gates and is expected to dissipate 8.8 W.

Functional simulation vectors have been generated for major circuit blocks within the chip using the STL (Simulation and Test Language) tool. This language allows behavioral modeling of the chip for the generation of expected response vectors given a set of procedurally generated stimulus vectors. These vectors have subsequently been used to simulate portions of the circuit using the SILOS logic simulator. Figure 15 shows an HCAD display of the functional simulation of the chip's 4-bit Cycle Counter.

Finally, HCAD's Timing Analysis tools have been run on the standard-cell design to isolate the pre-layout critical path which occurs within the multiplier. In addition, some initial work has been done with the layout tools to prepare for the automatic place and route of the Transversal Filter chip. This includes generation of larger 6 mil I/O pads, as well as placement files for the I/O cell instances. An initial chip layout should be available in the very near future.

2.2.9 Cell Array Design (W.B. Leung, E.K. Poon)

Two cell array designs, PT-2M 4 Bit Adder and PT-2L Quad 4 Bit Adder, were described in the last semiannual report. Based on the experience with those designs, we have decided to design a 1K cell array. This circuit is intended to fully exercise the CAD tools and the basic cells, which will also be used in the 5K cell array.

The 1K cell array has 1024 basic cells, 80 I/O buffers, and 48 power pads. The floor plan of the array is shown in Figure 16. Each basic cell can be personalized into an inverter, 2-input NOR gate, 3-input NOR gate, or 4-input NOR gate. Each personalization also has a high-drive option for signals having high fan-out or routing capacitance. The SFFL logic family was selected because they have been implemented successfully in PT-1. Provisions have been made to the basic cell, the I/O buffer, routing channels, and reference coordinates so that they are compatible with the MagicCAD system at Mayo Foundation.

The logic design is supplied by Mayo Foundation. It consists of a dual data path with counters, registers, multiplexers, comparaters, and a 6x6 multiplier. The total gate count is about 750, which corresponds to 73% utilization of the cell array. This design emphasizes testability, and many control signals are included so that each functional block can be tested. Also several of them can be connected together to determine the performance in a system environment. In the current design, it is possible to omit a very small part of the circuit and wire bond the chip into the Interamic 88 pin package, which allows for 64 signals. For designs with more than 64

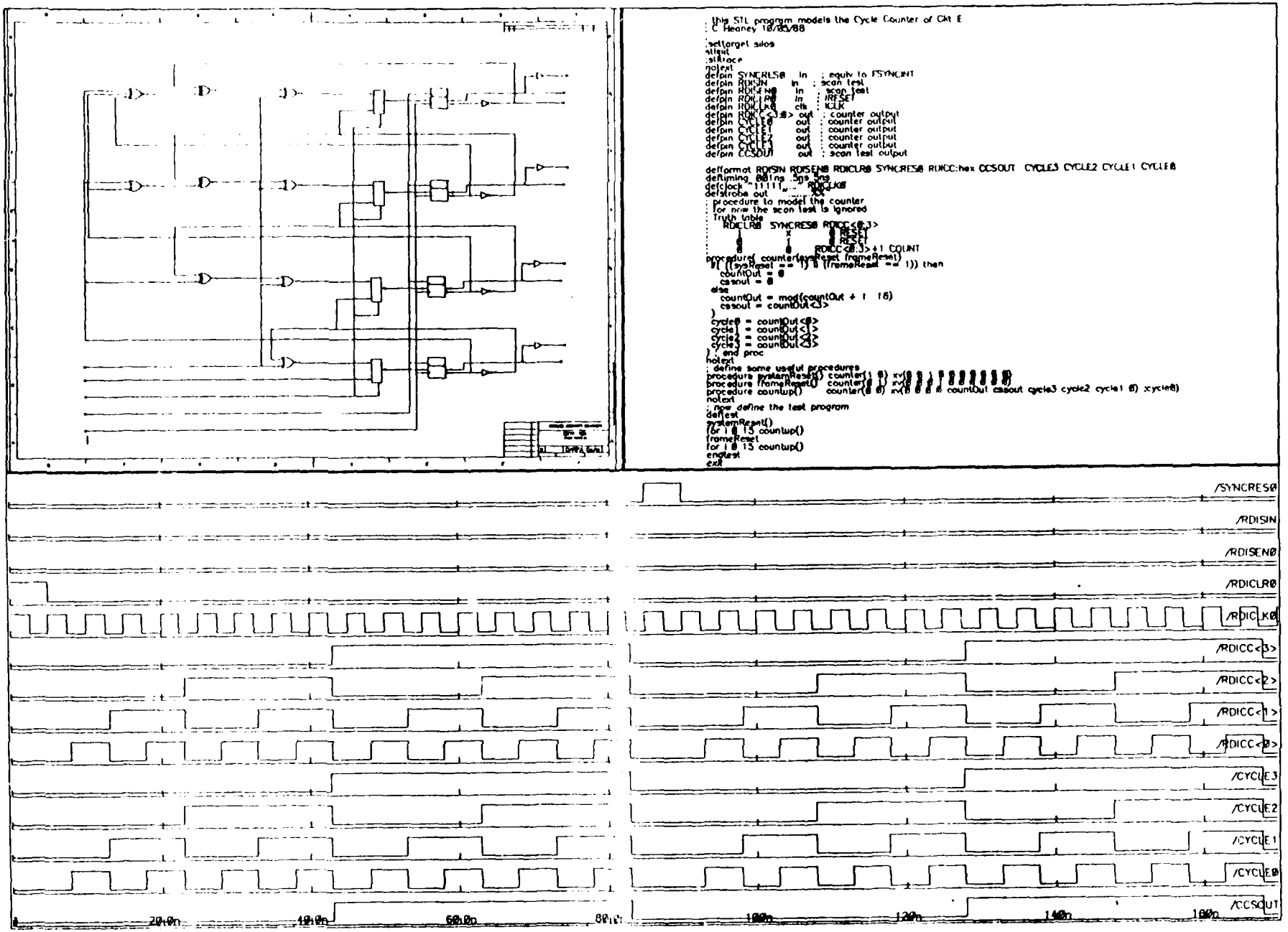


Figure 15. Cycle Counter HCAD Simulation.

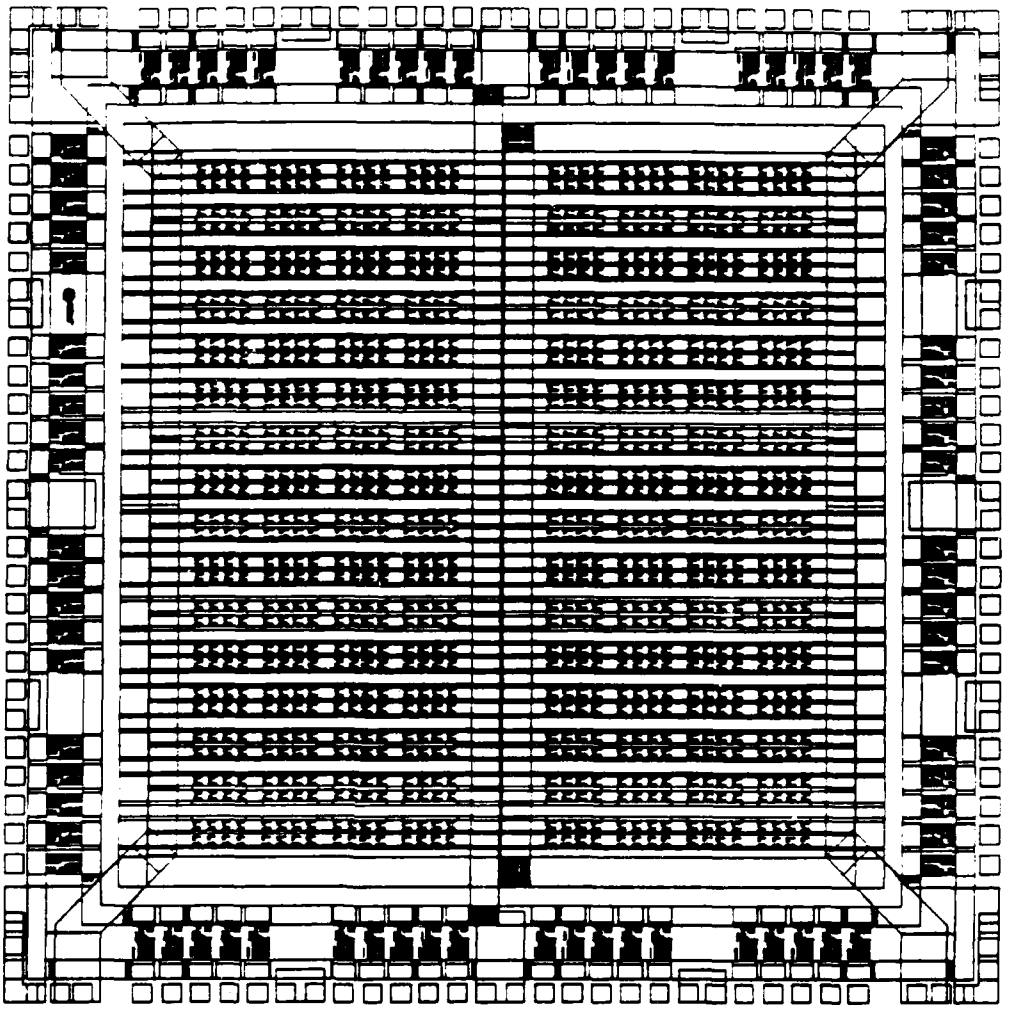


Figure 1. 1K Cell Array Floor Plan

Figure 16. 1K Cell Array Floor Plan.

signals, a larger package such as Rodgers Microtec P164 can be used.

First draft of basic cells, personalization schemes, I/O buffers and simulation data were sent to Mayo Foundation in August. The final version of the cell array, incorporating suggestions from Mayo, should be ready in early October.

2.2.10 Custom Circuit Design - ALU (K. W. Teng, Y. B. Leung, T. C. Poon)

The custom circuit A - 32 bit ALU is implemented as a test vehicle for very large circuits with close to 3.5 K gate complexity. Circuit A is intended to expand on the results of PT-1 as well as PT-2L, and to include better marginality as well as better performance in the circuit. This will enable the designers to exercise their CAD tools, and to further improve the modeling of circuit behavior, the process control over a large logic circuit, and the yield characteristics.

The logic design of circuit A was done by McDonnell Douglas Corporation, and it consists of the 32-bit ALU and two sets of 32 x 5 registers of a 32-bit RISC microprocessor. This ALU can perform nine functions: four logic and five arithmetic. It contains a 34-bit adder and a 32-bit logic unit. All logic operations are performed on 32 bit operands. The estimated die size, power consumption, and the transistor counts are shown in the following table. This circuit will demonstrate both processing and performance capability of the HFET technology and the SFFL logic family.

Input Signals	77
Output Signals	34
Logic Gates	about 3500
Transistors	about 24000
Die Size	6 x 6 mm
Estimated Power	3.1 W

Characteristics of Custom Circuit A - 32 Bit ALU

Various enhancements were added to this custom circuit to ensure fair circuit yield, high speed performance, low power consumption, and good reliability. These include the better optimization of noise margins with current technology, the implementation of faster as well as less process sensitive logic gate designs, and the suppression of the L DI/DT noise generated in the I/O buffers. In addition, with a divided routing/clock driver architecture (as shown in Figure 17), we are able to reduce the metal bus loading on the clock driver and to further

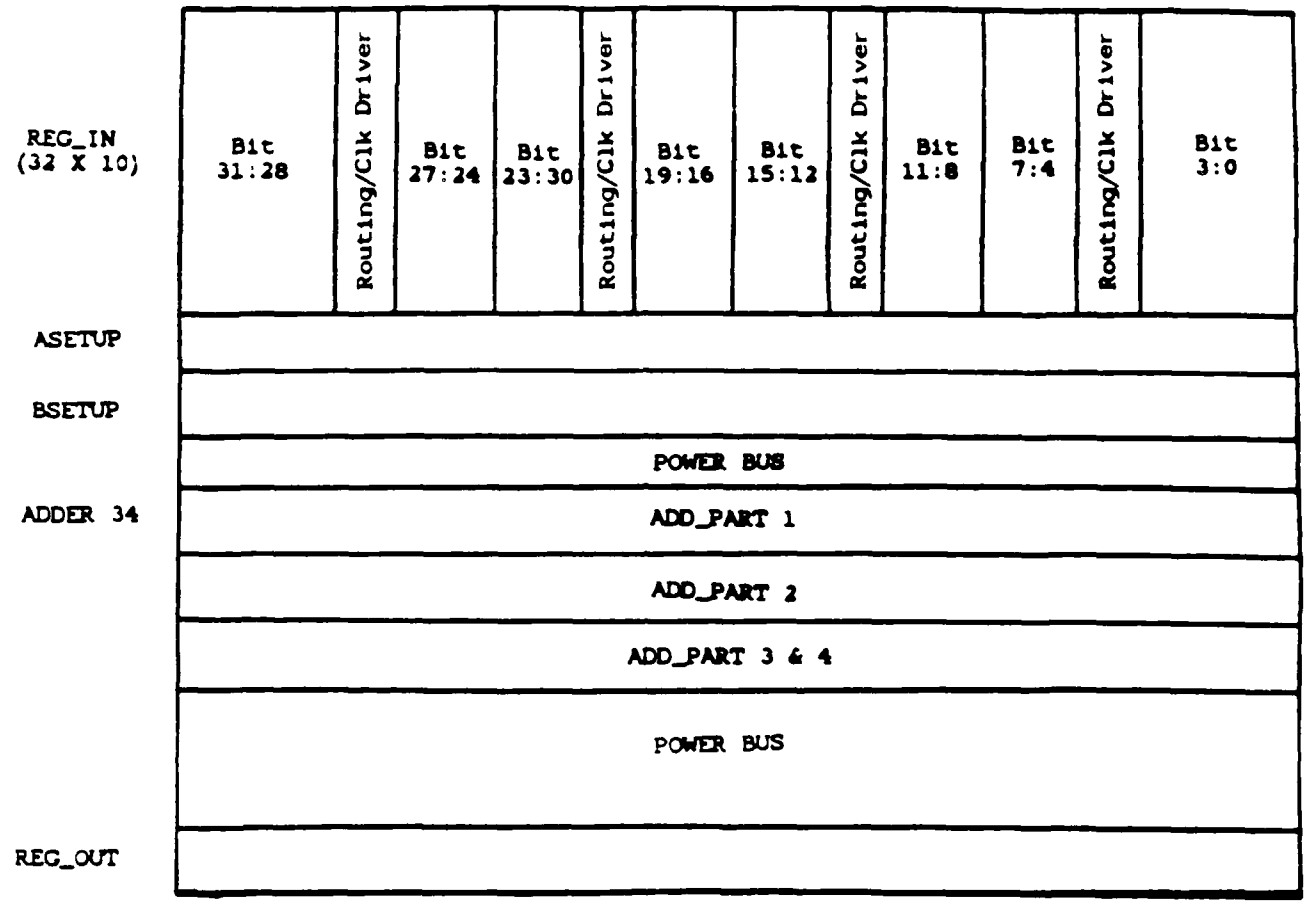


Figure 17. Custom Circuit A: 32-Bit ALU Layout Architecture.

enchance the circuit performance.

This ALU is designed with the gate-matrix technology. Layout of the circuit is then verified using the CAD tools such as: GASCHK, GOALSL, LLC, and MOTIS3. Pre-layout and post-layout timing simulations are studied including all critical path delay times. The pre-layout simulation results show that this circuit can perform very well to meet DARPA's Statement of Work requirements: 200 MHz operation, assuming a pipelined chip design with 15-20 cascaded gate delay stages, with each gate driving a load of at least three similar gates. The post-layout simulation results will be presented in the next report.

2.3 DESIGN TOOLS

2.3.1 Standard Cell and Macrofunctions (A. I. Faris)

A standard macrocell library consisting of 47 cells was designed and laid out in the 2μm SARGIC/HFET process. The cells will be used in Hughes Transversal Filter Chip. We are presently simulating the cells using the nominal device model parameters with AT&T's ADVICE circuit simulator. The macrocell library is an enhancement of the original standard cell library. Many commonly used functions are laid out as a single macrocell. Compared to an implementation using the original standard cells, a macrocell implementation results in lower power consumption, smaller chip size, and faster chip speed. The macrocells all have the same height, thereby avoiding the layout problems that occur when cells have different heights.

The following is a list of the macrocell library.

1. INRB, Inverter*
2. NR2, 2 input NOR gate*
3. NR3, 3 input NOR gate*
4. NR4, 4 input NOR gate*
5. NR5, 5 input NOR gate*
6. AOI22, AND/OR/INVERT 22*
7. AOI32*
8. AOI33*
9. AOI3333*
10. FADD, full adder
11. HADD, half adder
12. XOR, 2 input Exclusive OR gate*
13. XNOR, 2 input Exclusive NOR gate*
14. MUX21, 2 to 1 Multiplexer*
15. COMPB4, 4 bit magnitude comparator
16. DECB4, 4 to 16 bit decoder
17. SIGDRV, Non-Inverting Signal Driver
18. CKDRV, Non-Inverting Clock Driver
19. TBFIN, Non-Inverting Tri-state Buffer
20. FD1S2AX, Negative Edge Trig. D Flip Flop*
21. FD1S2DX, Negative Edge Trig. D Flip Flop with positive clear*
22. FD1S2NX, Neg. Edge Trig. D Flip Flop with pos. clear and preset
23. FD1S5F, Neg. Level Trig. D Flip Flop with pos. clear and preset
24. BIIO1, Inverting Input Buffer
25. BINO1, Non-Inverting Input Buffer
26. BO50, Non-Inverting 50 OHM output Buffer
27. BME, booth mult. encoder
28. BMMUXB4, booth mult. multiplexer
29. BMFAB4, booth mult. full adder
30. BMHAB4, booth mult. half adder
31. BCLAB4, block carry look-ahead adder
32. CLCB4, carry look-ahead circuit
33. CLAB4, carry look-ahead adder
34. REGFB44, 4 by 4 register file
35. BARSRB4, 4 bit barrel shifter
36. SRSIPOB4, 4 bit serial in parallel out shift register
37. SRPISOB4, 4 bit parallel in serial out shift register
38. SRPIPOB4, 4 bit parallel in parallel out shift register
39. SRMXPIB4, scan multiplexed shift register
40. CTRUB4, 4 bit synchronous up counter
41. CTRDB4, 4 bit synch. down counter
42. CTRUPB4, 4 bit synch. programmable up counter
43. CTRDPB4, 4 bit synch. prog. down counter
44. CTRUDB4, 4 bit synch. up/down counter
45. CTRUDPB4, 4 bit synch. prog. up/down counter
46. ALUB4, 4 bit arithmetic logic unit
47. ALUCLG, 4 bit ALU carry look-ahead generator

* These cells are dual gates in a cell

2.3.2 Parameter Extraction and Modeling (R. D. Pierce, J. L. Lentz, and P. G. Flahive)

In this report period we have issued sargicS FET models 6 through 12. We have extended our modeling strategy from a mode of tracking data to the use of device simulation to predict FET characteristics and to engineer material structures. Some key characteristics of versions 6 through 12 are shown in Figure 18. Earlier versions are also plotted for reference.

Versions 5 through 9 represent the older strategy of tracking FET data to extract model parameters. Version 5, issued in the previous report period, was based on PT-0 baseline FET data. Versions 6, 7, and 8 were evolutionary upgrades primarily involving the E-tub diode models. Version 9 was the first version to include best and worst case noise margin models. It was an engineering estimate based on the first PT-1 baseline wafer set, intended to simulate $\pm 1\sigma$ variations in EFET threshold voltage and E/D current ratio. Designer experience with version 9 showed that it was unacceptable. The EFET threshold voltage was too high, limiting high noise margins. The current ratio was too low, impacting circuit FET width ratios, and the threshold variation was too wide.

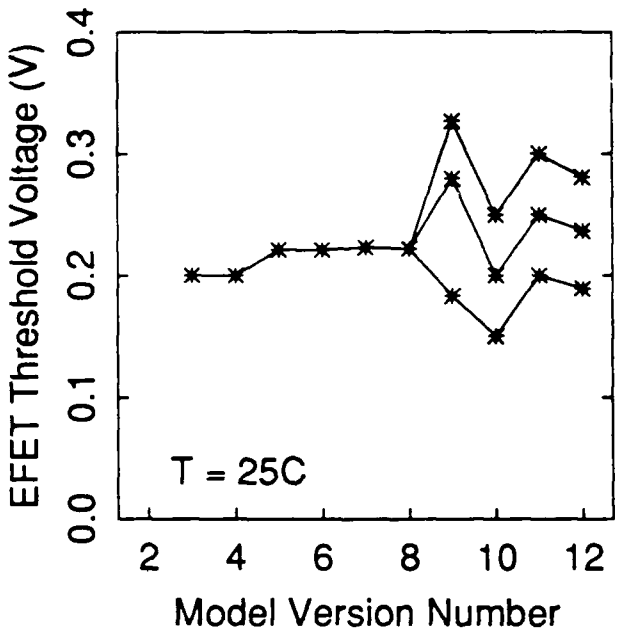
Versions 10 and 11 represent a strategy of response to design community needs. They addressed the shortcomings of version 9, iteratively introducing characteristics acceptable to the design community, and thereby establishing targets for material growth and device fabrication.

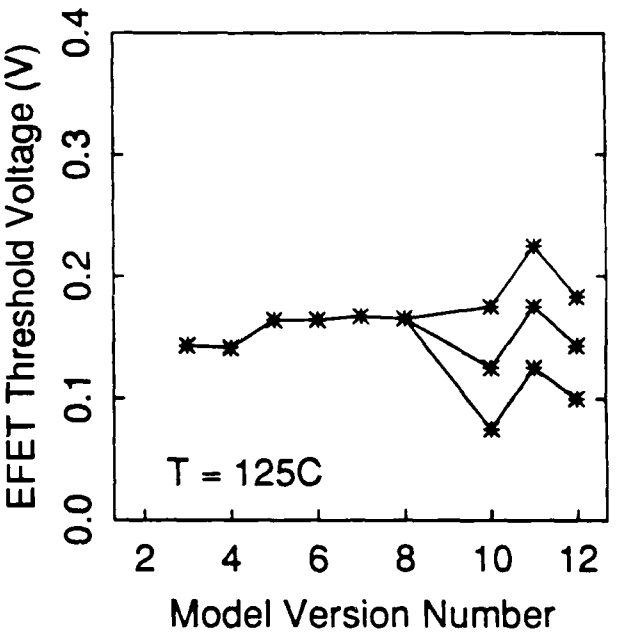
Version 12 adopts a strategy of material engineering and device simulation, using the one-dimensional device simulator SIGMA. SIGMA calculates the equilibrium charge distribution and band structure of a GaAs/AlGaAs heterojunction device at a given gate bias by self consistently solving Poisson's equation with Schrödinger's equation for the device. The band diagram and charge density as a function of depth for an EFET with characteristics matching the designer requirements are shown in Figure 19. The charge density under the gate is integrated to yield the sheet charge, Ns, from which threshold voltage can be extracted.

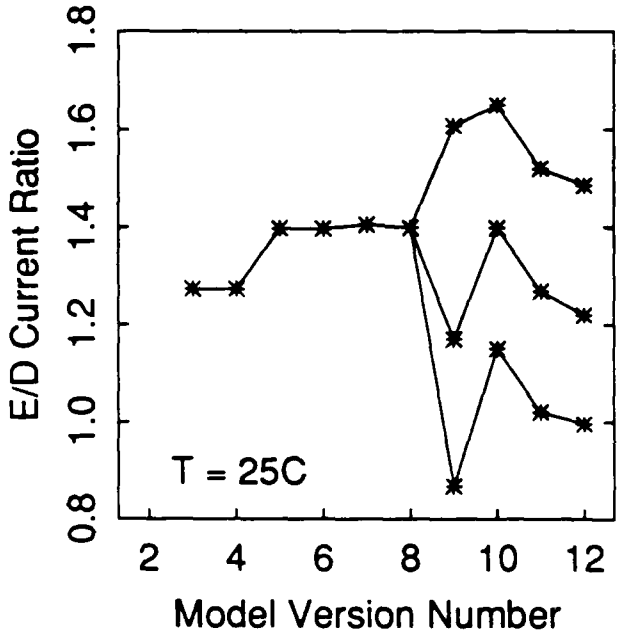
Simulated threshold voltages were compared to measured threshold voltages for two periods of MBE growth to establish correlation between simulation and measurement. A decrease in material layer thickness had occurred during one of these periods, resulting in a shift in threshold voltage. The measured and simulated threshold voltage shifts are 150±75 mV and 100±50 mV, respectively, for the EFET, and 370 ± 110 mV and 270 ± 100 mV, respectively, for the DFET. The agreement is within the range of error for the threshold voltage and RBS thickness measurements.

For version 12, we have also used the GADVICE FET model which incorporates SIGMA results in a straightforward way, and includes an improved capacitance model. The characteristics of version 12, shown in Figure 18, are similar to those of version 11. Version 12 will be refined and subjected to verification when FETs using the modified structure become available.

The following table compares the AC characteristics of versions 9 through 12 with measured data. Version 12 maintains good agreement for expected ring oscillator delays and shows improved agreement for small signal microwave characteristics such as f_T.







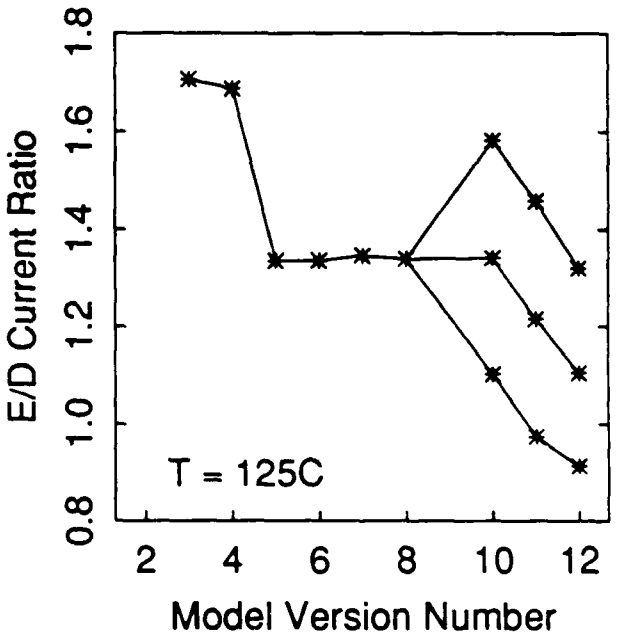


Figure 18. Comparison of sargicS FET Model Parameters.

SargicS.12 EFET

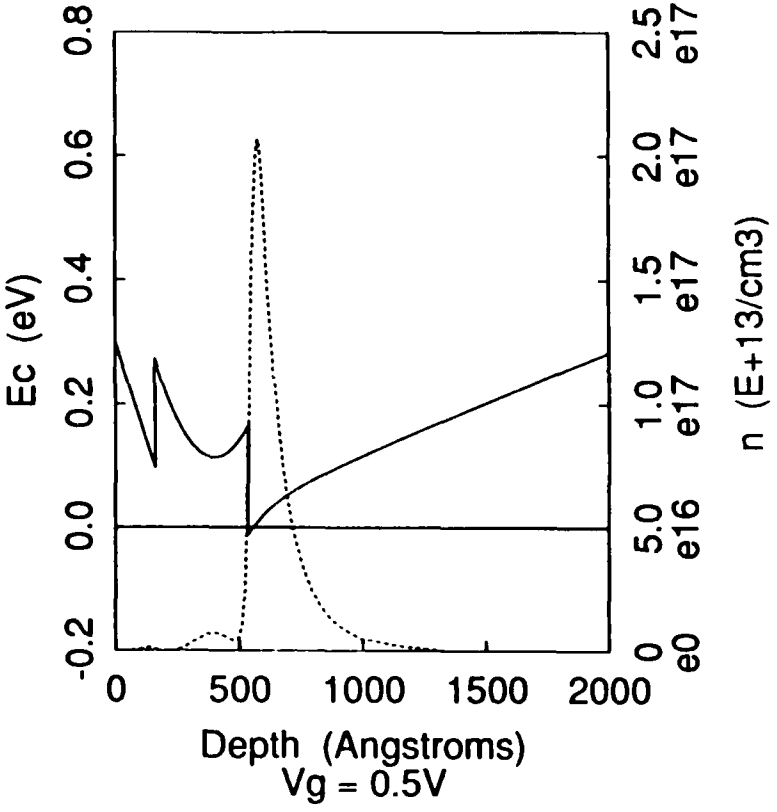


Figure 19a. Energy Band Diagram (Ec) and Charge Density (n) Used for the sargicS.12 EFET.

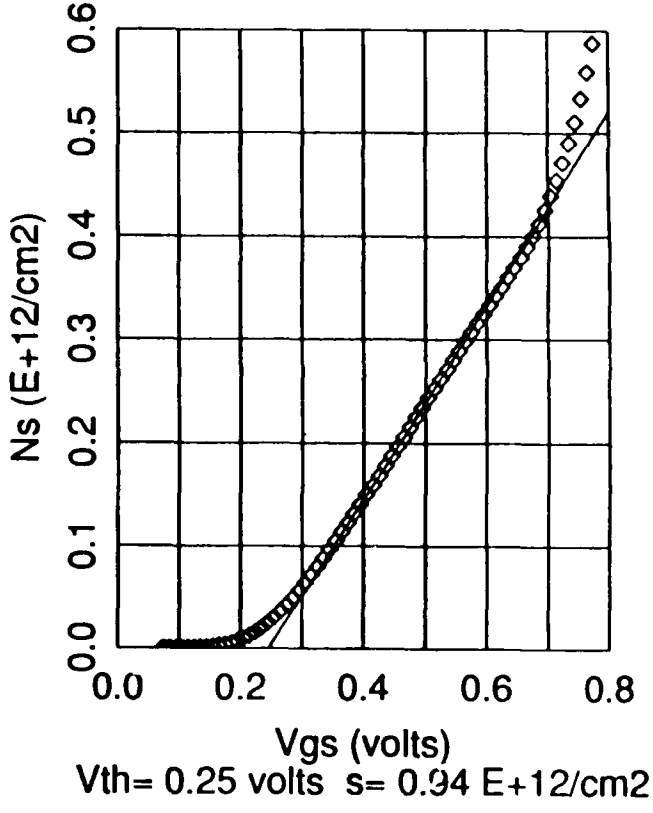


Figure 19b. Sheet Charge (Ns) Calculated for sargicS.12 EFET. The Diamonds are Data Points from the Calculation. The Line is a Best Fit which Extrapolates to the Threshold Voltage.

Parameter	PT-1 Baseline Wafers	sargicS.9	sargicS.10	sargicS.11	sargicS.12 (prelim.)	
R.O. Gate Delay (ps)	75-100	64	75	71	65	ps
Parasitic Load (fF)	---	5	5	5	5	fF
EFET f_T (GHz)	20-22	11.7	12.3	12.6	19.7	GHz
DFET f_T (GHz)	16-18	10.2	11.0	11.0	17.9	GHz

The sensitivity of threshold voltage to variations in material thickness and doping was also calculated using SIGMA, and the results are listed below.

Material Parameter	Sensitivity	
	DFET	EFET
Donor Layer Thickness	5.3mV/Å	2.6mV/Å
Undoped Layer Thicknesses	2.1mV/Å	1.8mV/Å
Doping	4.0mV/1E15cm^{-3}	1.4mV/1E15cm^{-3}

Threshold voltage is most sensitive to variations in the thickness and doping of the donor layer. These sensitivities imply that ±2% control of material variations is required to maintain threshold voltage within the ±50mV required by our current circuit designs.

2.4 Advanced Technology (R.H. Burton, A.G. Baca, K.W. Wyatt, A. I. Faris)

Several technology directions have been identified which will have a large impact on performance, and the advanced technology program activities will be focussed on these. Implementation of some or all of these features will allow us to achieve the program goals of demonstrating circuit performance of 400 MHz with 15-20 gate delays. Key areas of emphasis include a new design approach, reduction of design rules, a lower dielectric constant inter-metal insulator, and the 0.5μm single quantum well transistor (SQT).

Simulations on an advanced form of SFFL, whose circuit diagram is shown in Figure 20, offer the promise of enhancing the circuit speed to 400 MHz without any changes in processing. The advantages of the new SFFL are derived from the all-EFET push-pull output stage which dramatically reduces the charge and discharge times of the gate. Using this logic structure, a 3 input NOR gate with a fan out of 5 and with 25 fF of load capacitance provides a propagation delay (via simulation) of less than 100 ps. The advanced process tester APT-1 will incorporate ring oscillator testers which will be used to verify this expected performance while comparing the advanced SFFL with DCFL and FIL logic families. From PT-1 experience, good agreement has been seen (70 ps, simulated vs 78 ps, measured) between predicted and observed baseline technology ring oscillator performance. Hence, comparable simulation/measurement performance agreement is expected for the advanced technology SFFL.

Process development activities are underway to prove-in the new 1.5μm design rules. The photolithography process is undergoing optimization for the new design rules. Initial

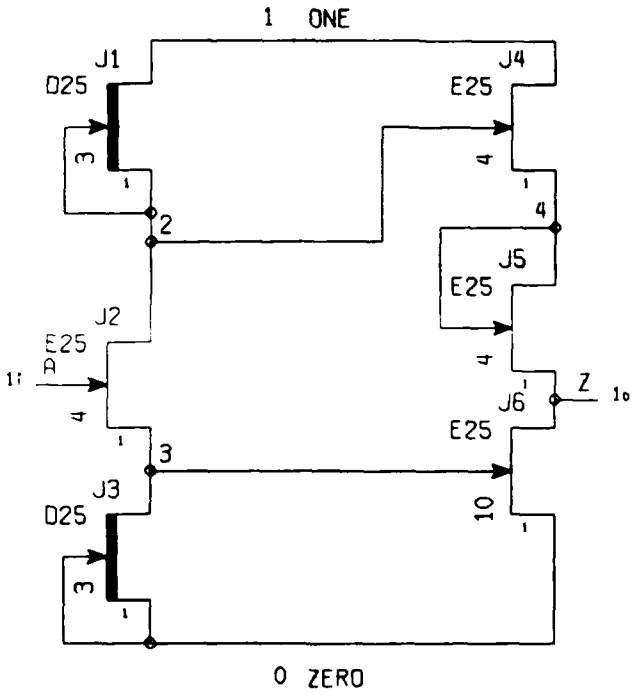


Figure 20. Advanced SFFL Inverter.

demonstrations exist for the via lithography and etch processes, but the overall process is yet to be defined. A full evaluation of the new design rules will be made when APT-1 processing commences next quarter. In addition, APT-1 includes testers (process and circuit cell) to evaluate various layout approaches which will afford additional compaction in layout if they can be successfully employed without adversely affecting Vth control or other desirable electrical characteristics. These include layout of interconnect metal over transistors, perpendicular gate orientations in the same layout, and direct connection of topmetal to gate or ohmic metal. Development of a planar interconnect process is a key aspect of achieving some of the layout compaction options. In addition, yield goals will be more easily achievable and the stepper photolithography process will be more manufacturable with planarization. The planarization process will focus on an approach including via plugs, for which, an initial demonstration exists, and dielectric etchback for smoothing the effects of metal morphology.

Dielectric activity will focus on SiO_2 to reduce parasitic capacitances. Because of reliability concerns, a thin SiN layer will be used to contact the GaAs surface. A demonstration of performance using SiO_2 was carried out with PT-1. Delays of 3-input nor gates with 1 mm of wire loading were reduced from 150 ps using SiON to 115 ps using SiO_2. Via and crossover testers showed no differences between SiON or SiO_2.

Implementation of the SQT is expected to provide greater noise margin over the military temperature range because of its better electron confinement. The SQT layer structure, illustrated in Figure 21, was chosen to achieve several objectives. The doping and thicknesses were chosen to give the same EFET and DFET currents as the baseline HFET to allow parallel processing of HFET and SQT. This lowers risk in implementing new designs, design rules, etc. The EFET structure contains undoped GaAs and 50% AlGaAs layers in order to increase the turn-on voltage and improve noise margins, potentially making DCFL viable. Simulations have shown that the redesigned buffer region optimizes carrier confinement and simplifies MBE growth. Parallel development paths using 0.75 and 0.5μm gates will be carried out. It is anticipated that a 0.5μm gate process using an optical stepper can be achieved by mid 1989.

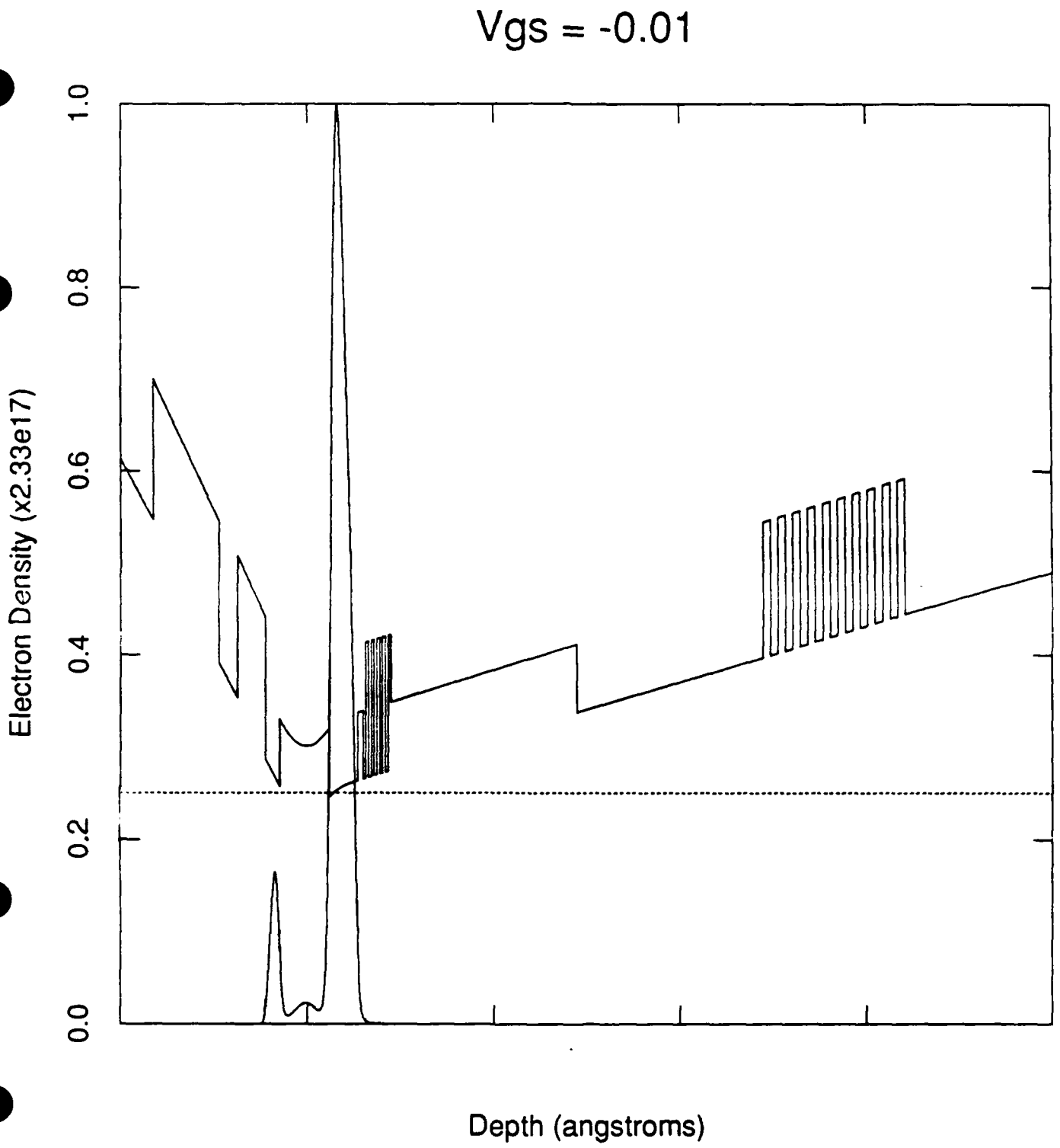


Figure 21. SQT Energy Band Diagram.

3. PILOT PRODUCTION

3.1 Pilot Line Throughput, Interval and Yield (V. N. Patel)

In this semiannual period, 371 wafer starts were made in the Pilot Line using PT-1, PT-2L and the Casino Test Chip. There was also additional wafer fab for internal and commercial customers. Wafer starts have been averaging 20 to 30 wafers/week for all starts. For PT-1, PT-2L, and the Casino Test Chip, Figure 22 shows wafer starts and completions shipped for PCM testing. The following table summarizes wafers completed and shipped by circuit for PCM testing.

Wafer Fab Activity, April through September, 1988

Recticle Set	Started	Shipped to Test
PT-1	303	280
PT-2L	32	3
Casino Test Chip	36	4
	371	287

Wafer Fab Activity, October 1987 through March 1988

PT-0	109	102
PT-1	195	--
	304	102

In order to minimize inventory and improve turnaround time, wafer starts have been limited to focus attention on output. A management team was formed to review inventory and interval weekly. Figure 23 shows significant decrease in the wafer processing interval from ~100 working days in December 1987 to ~45 days in September 1988.

Down time on the arsenic over pressure anneal furnace tube and the Nikon Stepper coupled with increased wafer starts in third quarter, 1988, increased the processing interval. Interruptions in product flow associated with the marginal processing capability of the anneal furnace continues and Engineering is evaluating vendors for a new furnace facility. Process development is continuing in order to explore the possibility of using Rapid Thermal Annealing instead of the furnace anneal.

Via etch, passivation etch and ohmic evaporation operations previously performed in another clean room have been moved into the Pilot Line. In addition, orders were placed to purchase a second Nikon Stepper, and an SVG alloying facility. Both will be proved-in by March, 1989. In addition, a second test set will be placed in service by March, 1989, to increase test set capacity for PCM testing.

Figure 24 shows PT-1 data for monthly and year to date wafer throughput yield (wafers ready for PCM testing compared to wafers started in the fab line). The decrease in yield in the last few months is partially due to the introduction of screening criteria for electrical parameters in addition to the existing mechanical criteria. In addition, several lots were scrapped in June at different operations as inspections highlighted processing flaws. In September, several lots were removed form the line as a result of screening for threshold voltage at ohmic test. These

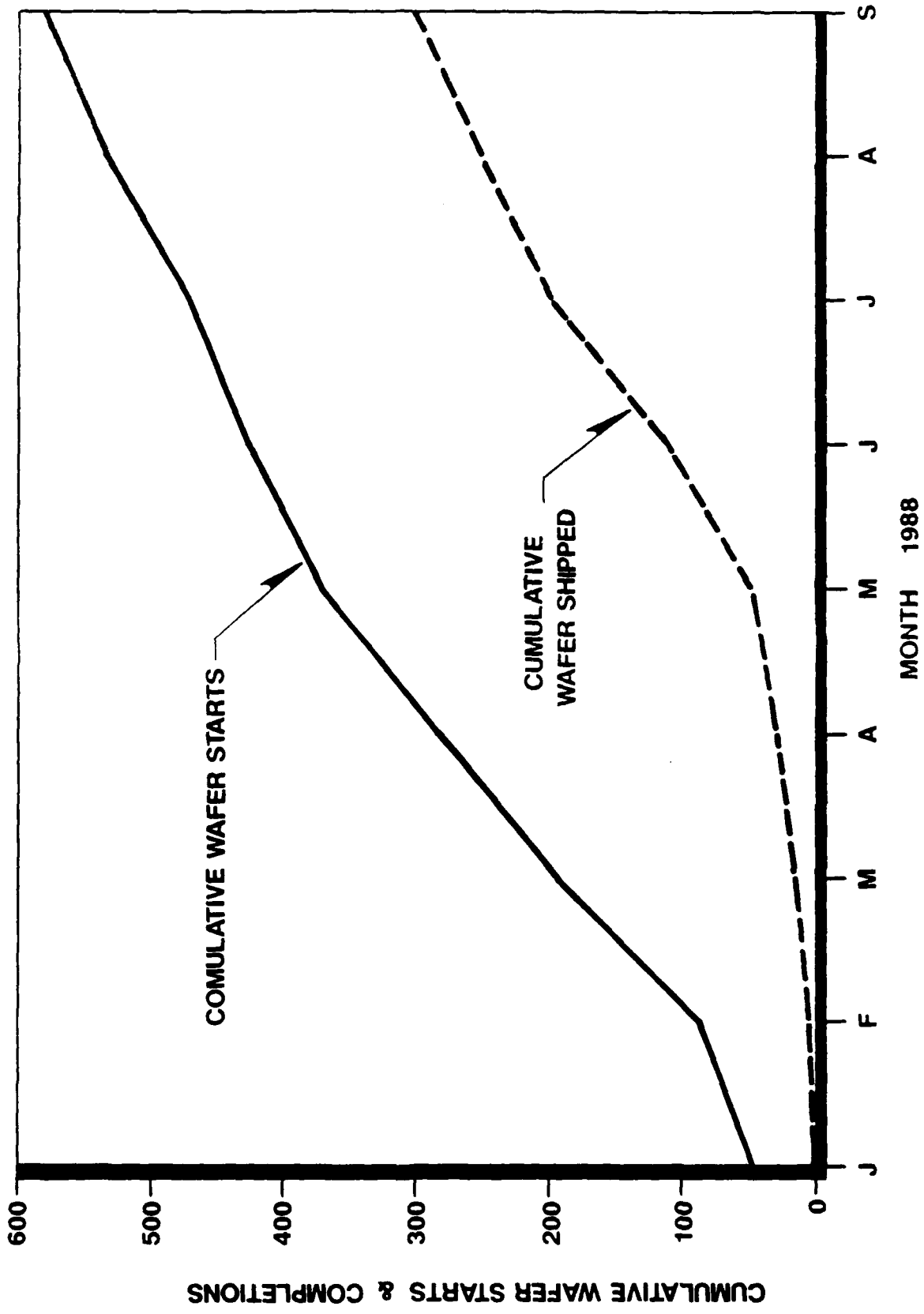


Figure 22. Pilot Line III Cumulative Wafer Starts and Completions for Calendar 1988.

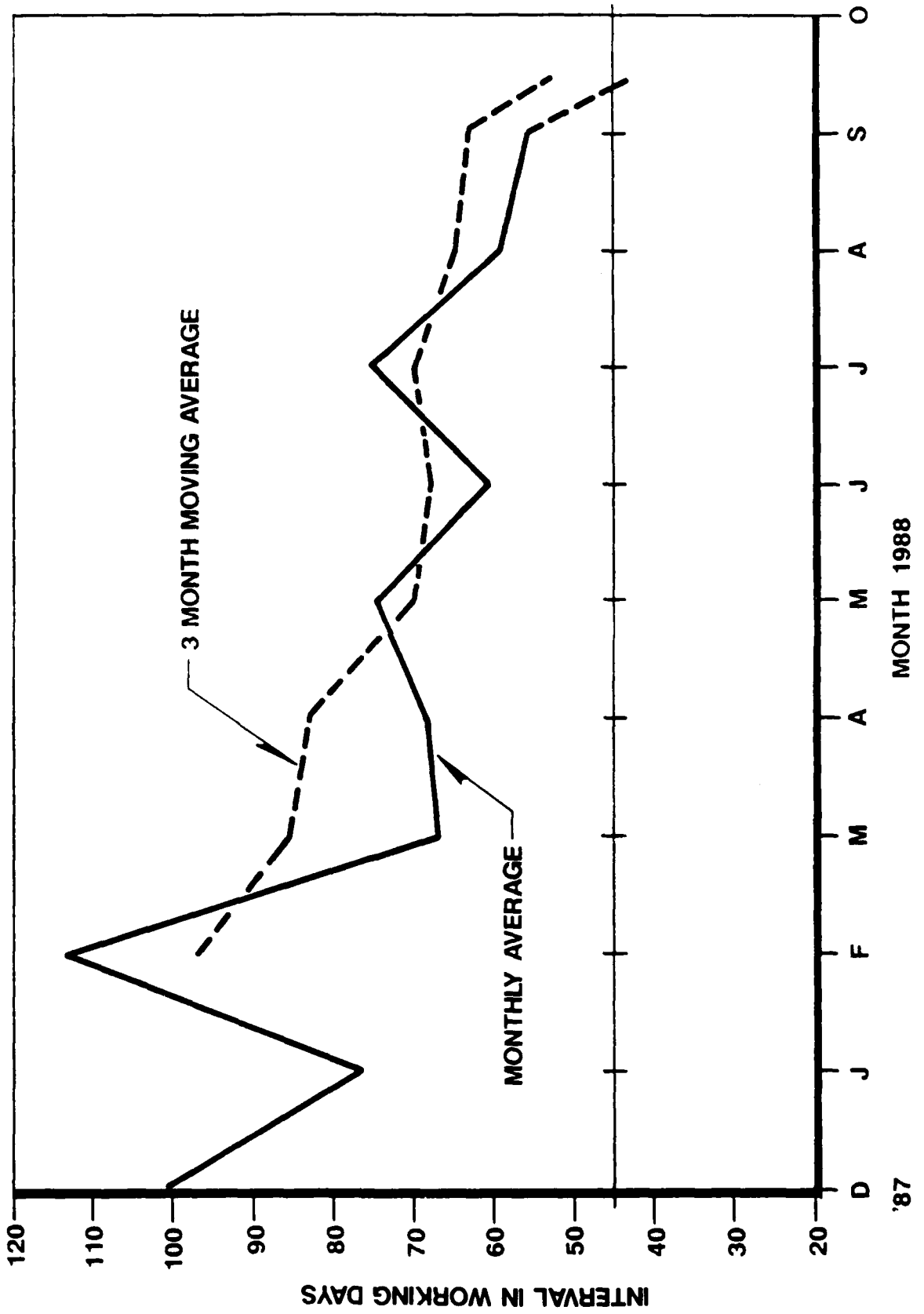


Figure 23. Pilot Line III Process Interval.

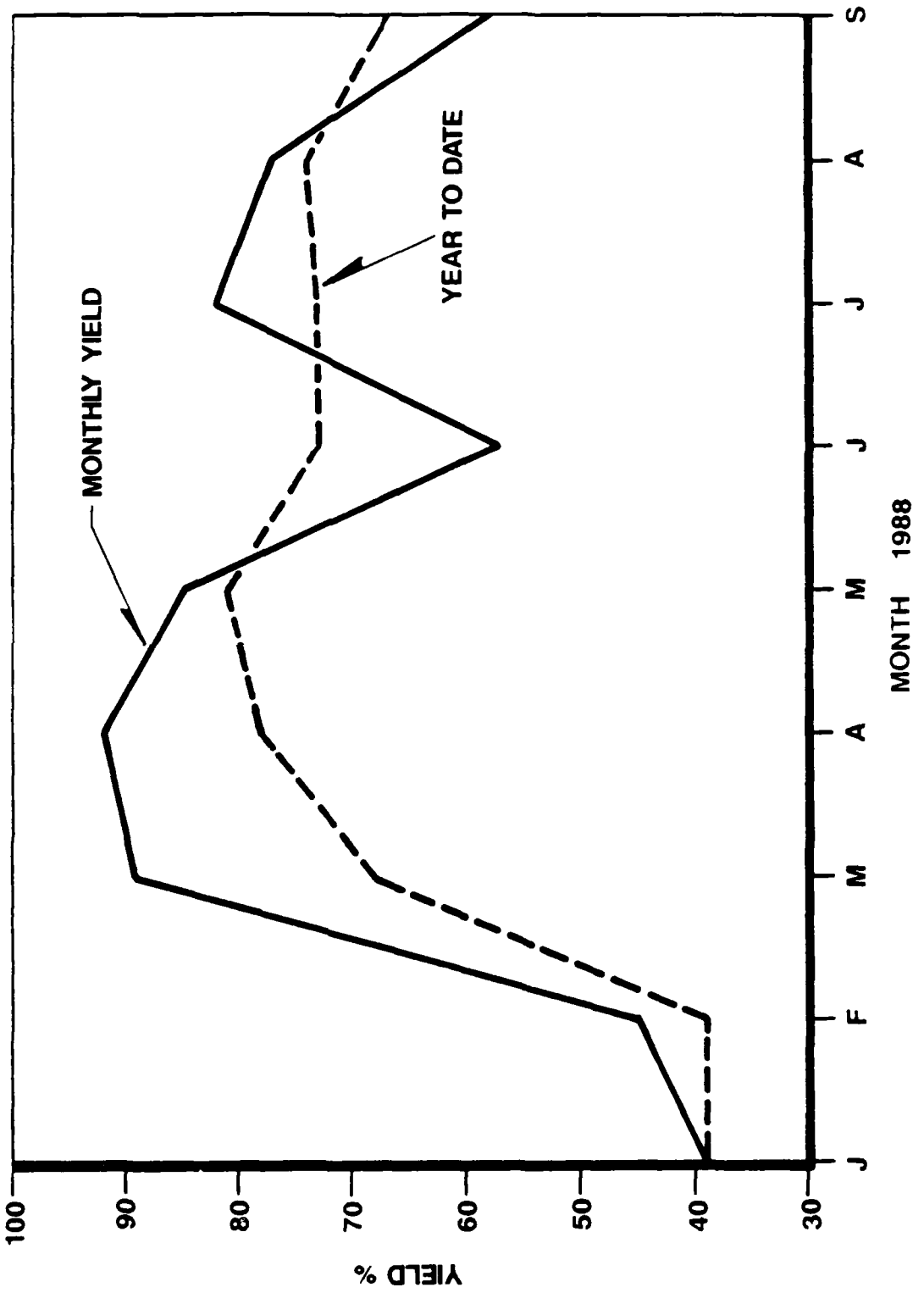


Figure 24. PT-1 Wafer Throughput Yield.

lots also had GaAs particulate redeposition during the furnace anneal. Finally, 3 lots had to be scrapped at E gate etch as the pH for the etch was improperly recorded due to a faulty pH meter. Long term throughput yields have averaged over 75%.

3.2 MBE (J. M. Parsey)

Several milestones were reached in this period. At the end of this six months, six hundred and thirty four wafers have been delivered to the processing line. A total of eight hundred and fifty-one wafers have been delivered cumulatively his year. The facility has surpassed a total output of more than two thousand wafers. The #1 MBE apparatus reached nearly a full year of operation without a major mechanical problem. The #2 MBE apparatus was staffed to two shift operation, bringing the output of the facility to 48 wafers per week. Additional work on utilizing larger sources for deposition has permitted operating the machines for 40-50 days between recharging and recalibration. This is in contrast to the 20 day cycle experienced with smaller source volumes. As a result, the total output of the two machines can be sustained in the range of 48-56 wafers per week. The greater number represents the addition of the larger sources: experience with the larger sources is still being acquired. A third Varian modular GEN-II machine was purchased and emplaced in September. Installation of liquid nitrogen lines is proceeding at the present time to supply sufficient LN_2 for this unit.

We have learned that the machines can be restored to a consistent state of operation in roughly ten days, inclusive of calibration and evaluation time. Attempts to shorten this cycle have been unsuccessful. Using the Hall-effect, SEM and cathodoluminescence, and Rutherford Backscattering (RBS) measurements, we have been able to restore the machines to the same operating state within a small window, roughly ±20-25Å total thickness variation in the Pilot Line III HFET structure, and a measured carrier concentration of $1x10^{12}$ cm^{-2}, ± ~10%.

We have found that the machines can be controlled to be highly reproducible following a recharge and recalibration. However, the absolute calibration lies within the 20-25Å window noted above. It has been suggested that this level of control may be insufficient to achieve consistent device characteristics. To better understand the variation and capabilities of the MBE growth process, extensive Failure Mode Analysis is in progress on archival material grown during the past year. Transmission electron microscopy is being used to determine if a measurable variation or variability in thickness actually exists. For electrical evaluation we are presently limited by the accuracy of the Hall-effect measurement.

Efforts have been directed to improving our ability to better measure the layer composition, thicknesses and carrier concentration, and to assure a more exact restoration of the operating conditions. To this end, new methods for characterizing the multi-layer structures by electrical and optical means are being evaluated, e.g., electron beam electroreflectance, eddy current coupling, photoreflectance, and photoluminescence.

3.3 Baseline Technology (R.H. Burton, A.G. Baca)

The baseline technology process remains essentially the same as that described in the previous report, although a number of process steps have been improved and are potentially yield

enhancing. The reproducibility of the pre-gate AlGaAs removal etch was improved by automating the etch. Before introduction of the automated process, etching was inconsistent near the center of the wafer (though consistent near the outside), as monitored by the E-D step height. After introduction of the automated etch, the E-D step height uniformity improved, as did V_{th} uniformity. Via yield has improved for testers with morphology. Failure Mode Analysis indicated that WSi adhesion problems were responsible for initial low yields on the via1-via2 tester. Improving the oxide removal prior to gate deposition resulted in better adhesion of WSi and a factor of three improvement in the via1-via2 yield. A preliminary evaluation of a via plug process shows promise for further improving the via yield by improving step coverage of evaporated metal in via holes.

Particulates on WSi gates have been observed by SEM and TEM measurements after the furnace annealing. The particulates have been identified by Auger microanalysis as GaAs and are not visible by routine optical inspection. The GaAs particles result from a temperature gradient between the cold and hot zones of the furnace, allowing some of the wafers to sublime GaAs when the As flow is shut off. A solution to the problem requires elimination of the temperature gradient or implementation of a cap to the furnace anneal process.

Gatelength control has been monitored by means of a split cross bridge and is shown in Figure 25. Optical lithography with a single frequency light source and a reflective (WSi) substrate places stringent requirements on photoresist thickness in order to minimize linewidth variation due to diffraction effects. Control of the process has been improved primarily by reducing the thickness variation of the photoresist for gate lithography.

Sidegate susceptibility of the SARGIC HFET devices has been characterized, and process modifications are being investigated to reduce its impact. Figure 26 shows the effect of sidegate voltage on Idss with a 2μm sidegate spacing. Recent work has shown that by extending the implant isolation through the superlattice buffer, sidegating is reduced to a considerable extent, as shown in Figure 27.

3.4 Packaging of Specific Circuits (K. J. Brady, R. S. Moyer)

PT-1

A total of 496 devices have been packaged in the 44 I/O package from TriQuint. All chips were epoxy die bonded. A group of 45 of these packages was subjected to an in-house package qualification test series. The packages passed all tests except internal water vapor content, but this problem will disappear when the eutectic die bonding is used and the packages are hermetically sealed.

A total of 117 memory and more than 150 logic devices packaged in the 44 I/O package have been tested in the high frequency test fixture from TriQuint. A minor modification of this test fixture was implemented in order to make the package positioning easier

The trim and form tool for mounting the chip face up was received but it is not being used. Instead, a trim and form tool from another project for mounting the chip face down is being used. This tool does not produce an exact match to the test fixture and so a new trim and form tool has been ordered from TriQuint.

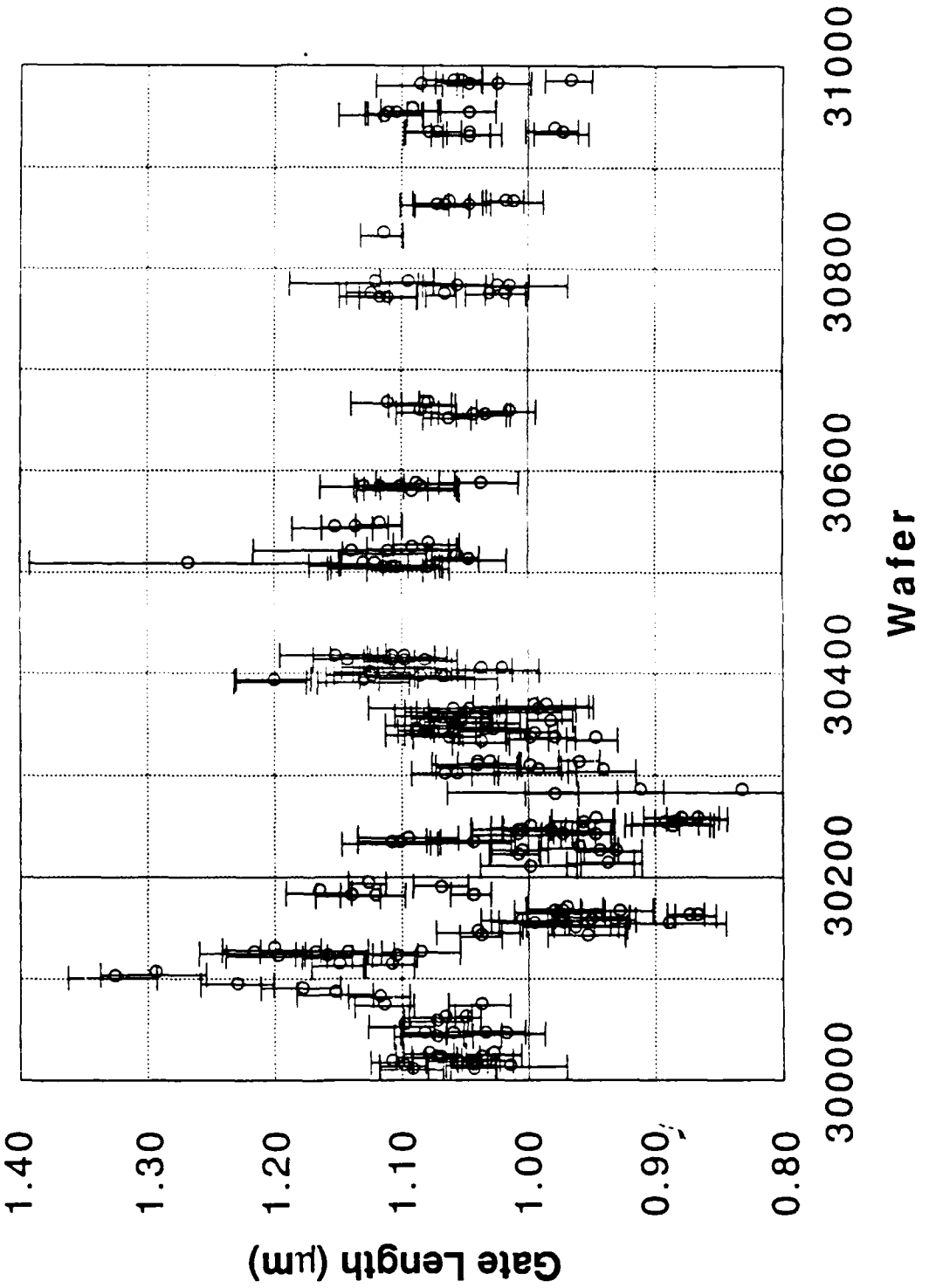


Figure 25. Gatelength Process History.

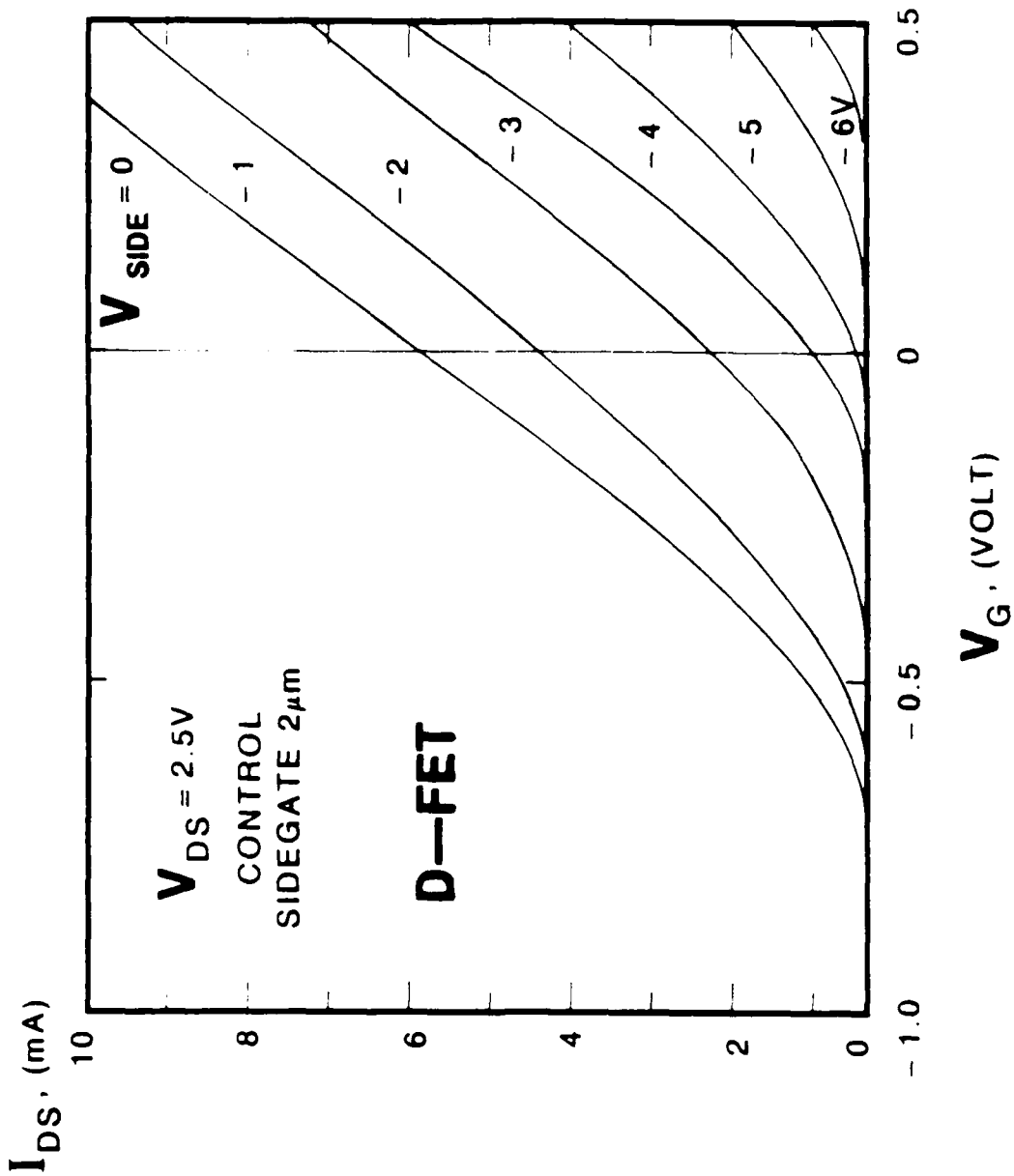


Figure 26. Effect on I_{DS} of a Sidegate with 2 μm Spacing.

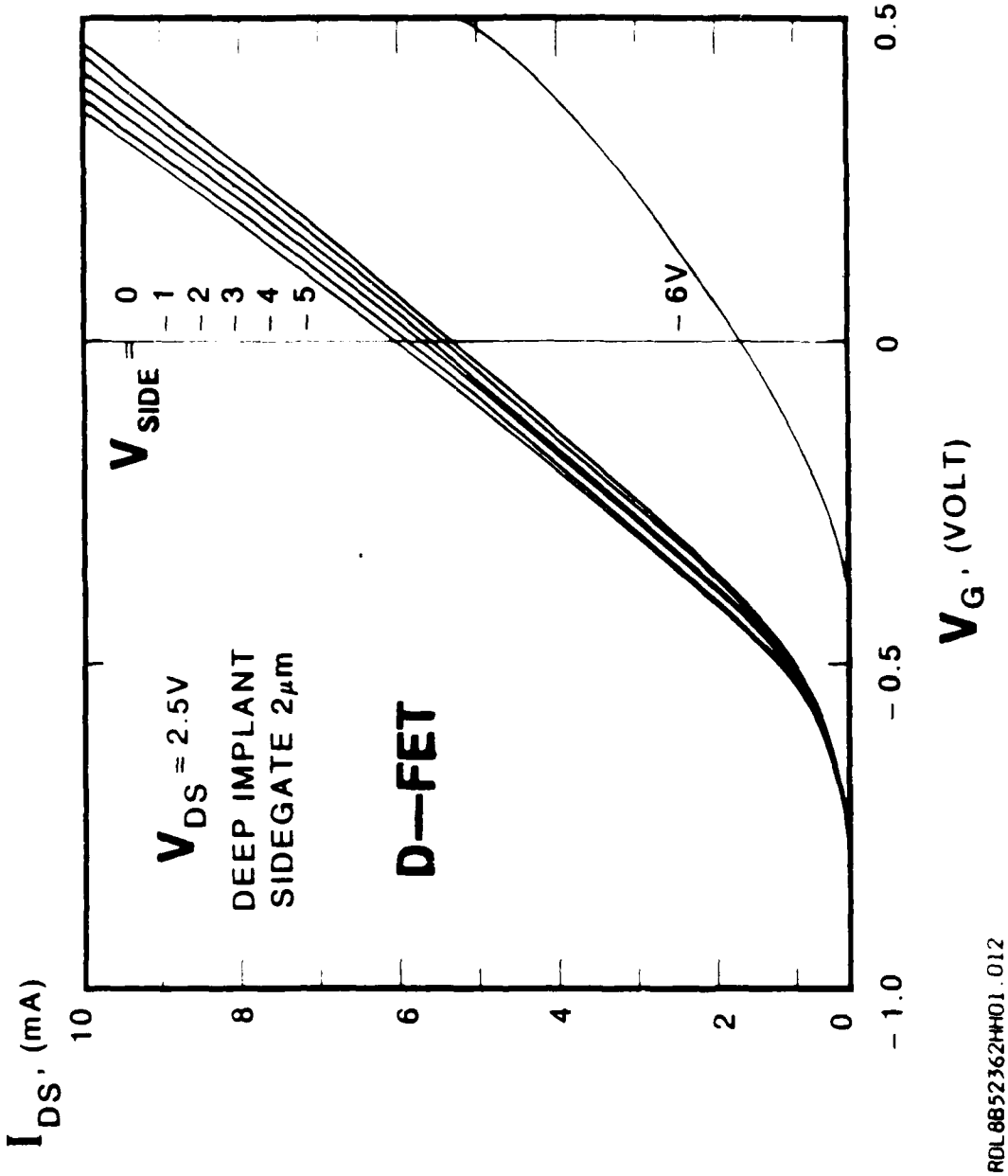


Figure 27. Effect on I_{DS} of a Sidegate with 2 μm Spacing.
Sidegating is Reduced by Extending the Implant Isolation Through the Superlattice Buffer.

PT–2 (Memory), 4K SRAM

The PT-2 memory chips have been laid out to be an exact match to the 44 I/O package, but none have been packaged yet. The current size estimates for the 4K SRAM indicate that it will not fit the 44 I/O package, but it will fit the 88 I/O package from Interamics.

PT–2 (Logic)

The order for 100 pieces of the 88 I/O package has been received. The purchase order for the low frequency carriers/sockets has been placed, and delivery is promised in January. A high frequency test fixture for this package has been built and tested. The Time Delay Reflectometry (TDR) measurements on the package/fixture combination indicate that it is superior to the TriQuint package/fixture combination.

The leads on this package will be left flat, so a trim and form tool is unnecessary.

Casino Test Chip

The AT&T designed 256 I/O fine pitch ceramic flatpack was approved for use with this chip. One hundred of the packages have been ordered, and delivery is due in mid-October. A group of 20 of the packages and lids (from internal supply) has been sent to Hughes Aircraft to package the first chips. Approximately 20 of the low frequency socket/carriers are on hand.

The high frequency test fixture for the 88 I/O package was modified to evaluate the electrical performance of this package. These tests are currently underway.

The leads on this package may be either trimmed short and left flat or trimmed and formed to a chip face up configuration; the socket/carrier can be modified to accept either. At this time there are no plans to build a high frequency test fixture for this package.

Transversal Filter Chip, Custom ALU and 1K Cell Array

The 164 I/O package from Rodgers Corp. (previously Augat-Microtec) is a good candidate for packaging these chips. It is a true high frequency package with controlled impedance signal lines, a high thermal conductivity die attach substrate and provision for mounting bypass capacitors on the package. However, because of its construction it is not hermetic and we will have to investigate its high temperature capability.

Azimuth Electronics has a socket/carrier tooled to accept this package with flat leads.

The high frequency performance of this package was evaluated in the modified 88 I/O test fixture. The TDR measurements indicate that it is as good as the 88 I/O package.

Summary of Package/Circuit Assignments

A summary of our proposed package/device assignments is given in the following table.

DARPA PILOT LINE III
PACKAGE-CIRCUIT ASSIGNMENT SUMMARY

Package	Pitch / Z_0	Signal Leads: Total Leads	Cavity Size: Max Die Size	High Speed Fixture Available	Burn-in Sockets Available	Circuit: Reticle Date	Die Size	Signal Count: Total I/O	Number of burn-in Sockets Required	Number of High Speed Fixtures
Tri-Quint PK-MLC-44-S	.050" 50Ω	24 44	.130" SQ .090" SQ	Yes TriQuint	Yes JEDEC	PT-1 11/87	.060" SQ	24 44	0	
						PT-2M 10/88	.080" SQ	16 44	11	
Interamics 64/88	.020" 50Ω	64 88	.250" SQ .210" SQ	Yes In House	2/89 Azimuth Elect.	PT-2L 6/88	.204" SQ	64 88	0	
						4KSRAM 12/88	.216" SQ	30 44	300	
NTK/256 Pin EMSP Package	.020" 58-66Ω	224 256	.560" SQ .520" SQ	No In House	Jan.'89 Yamaichi	Casino Test Chip 6/88	.327"x.337"	172 241	21	
Rogers/Microtech P-164	.025" 50Ω	148 164	.400" SQ .360" SQ	No In House	2/89 Azimuth Elect.	Transversal Filter Chip 3/89	.350" SQ	103 164	21	
						Custom ALU 1/89	.250" SQ	111 160	300	
						1K Cell Array 1/89	.212" SQ	80 128	21	

3.5 Configuration Management (R. L. S. Kotzmann)

Transmittal of manufacturing information for PT-1 from AT&T Bell Labs to AT&T Microelectronics at Reading, was achieved on March 31, 1988, with the completion and delivery of the attendant LDI (Laboratory Design Information - a company mechanism for transmitting manufacturing information from the design organization to the manufacturing organization) along with 98 drawings and specifications, which constituted the required manufacturing documentation for the GaAs foundry operation.

As is custom, these drawing were reviewed for manufacturing acceptability by the cognizant AT&T-Microelectronics manufacturing engineers, resulting in some minor changes to the Laboratories provided drawings and specifications. Subsequent approval by all parties resulted in the issuance of official manufacturing documentation on August 5, 1988. These official drawings and specifications form the basis for production of the Pilot Line III circuits. No production deviations can be made without going through a change control procedure. The change control procedure (configuration management) provides for two types of changes - one temporary and one permanent.

The mechanism for implementing a temporary change, one that does not result in a drawing change, is the issuance of a duly approved TIM (Temporary Information Memorandum). With the issuance of a TIM, product may be manufactured in accordance with the authorized deviation/s as specified in the body of the document - the TIM. Generally, TIMs are issued to evaluate a possible change or to allow a temporary substitution of a material used in production. Data obtained from these authorized temporary deviations may become the basis for an approved change to the documentation, and thus, be reflected in the product henceforth.

The mechanism for implementing a permanent change, one that results in changes to applicable manufacturing drawings and/or specifications, is the issuance of a duly approved Change Order (CO). Change Orders affecting Pilot Line III- related documentation will be assigned numbers from the 9000-9999 series for ready identification.

Appropriate logs will be maintained on TIMs and COs to facilitate configuration management control.

4. RELIABILITY AND QUALITY

4.1 Radiation Hardness Testing (M. Spector, S. D. F. Jones, S. B. Witmer, and R. L. Remke)

Total dose radiation experiments were completed on PT-1 HFETs, ring oscillators, and 256 bit SRAMs. They were exposed to gamma radiation from a Co^{60} source up to a dose of $6x10^8$ rad (GaAs). The SRAMs were irradiated with and without bias and all devices were periodically tested, visually inspected, and photographed under a high magnification microscope. After $1x10^8$ rad (GaAs), all devices showed very small changes in electrical characteristics (~5%). No significant differences were observed between the biased and unbiased SRAMs.

Transient ionizing dose testing was performed on HFETs, ring oscillators, inverters, and SRAMs. Transient dose testing of HFETs showed a photovoltaic signal with the source and drain nodes grounded and no bias applied. The HFET response is presently being modeled for use in circuit simulation of transient dose effects. Testing of ring oscillators and inverters showed that they recovered promptly after the radiation pulse at dose rates less than $1x10^{10}$ rad(GaAs)/sec. The SRAMs tested had low noise margins which contributed to the large number of bit errors (5%-10%) at dose rates less than $1x10^9$ rad(GaAs)/sec and also to the row and column failures. By masking out the marginal cells, a threshold of $1x10^9$ to $2x10^9$ rad(GaAs)/sec was observed in two devices. The transient response of the SRAM was also measured by connecting the DATAOUT line to a transient digitizer and placing the memory in the read mode. These measurements show that some cells are not toggled by dose rates as high as $1x10^{10}$ rad(GaAs)/sec.

Single Event Upset (SEU) measurements were made on Standard and Rad-Hard memory cells (256 bit SRAM) using the electron beam source at NOSC (Larry Flesner). These measurements showed an error rate of about $5x10^{-8}$ errors/bit day for the Rad Hard cell and about $2x10^{-7}$ errors/bit day for the Standard cell. The testing also showed that the most sensitive area for both types of cells was the area between the drain and source of the off driver FET of the memory cell (see Figure 28). Comparison of the experimentally observed error rates with analytical expressions for the error rate suggests that the HFET collection depth is less than previously reported values for GaAs devices. This reduced collection depth is believed to be due to the superlattice below the HFET.

4.2 Reliability (Y. L. Cho and R. L. Remke)

In continuation of the electromigration study on the PT-0 REM (Reliability Evaluation Module), further experiments were performed on the Ti/Pt/Au metallization system. To establish the activation energy and the n-factor involved in the electromigration process, we used the TRACE method (Temperature-ramp Resistance Analysis to Characterize Electromigration - R. W. Pasco and J. A. Schwarz, 1983 IEEE Intl. Reliability Physics Symp.). The results yielded an activation energy of 0.43 eV and an n-factor of 2. Additional electromigration aging tests were conducted at various temperature and current density levels, using a failure definition of any change exceeding 10% from the original resistance value of the sample. Combining the results, an expression for median time to failure (MTF) in hours was obtained:

$$MTF=2x10^{11}J^{-n}\exp\left(\frac{E_a}{k_BT}\right)$$

where J = current density (A/cm^2), n = 2, E_a = activation energy=0.43 eV, k_B = Boltzman's

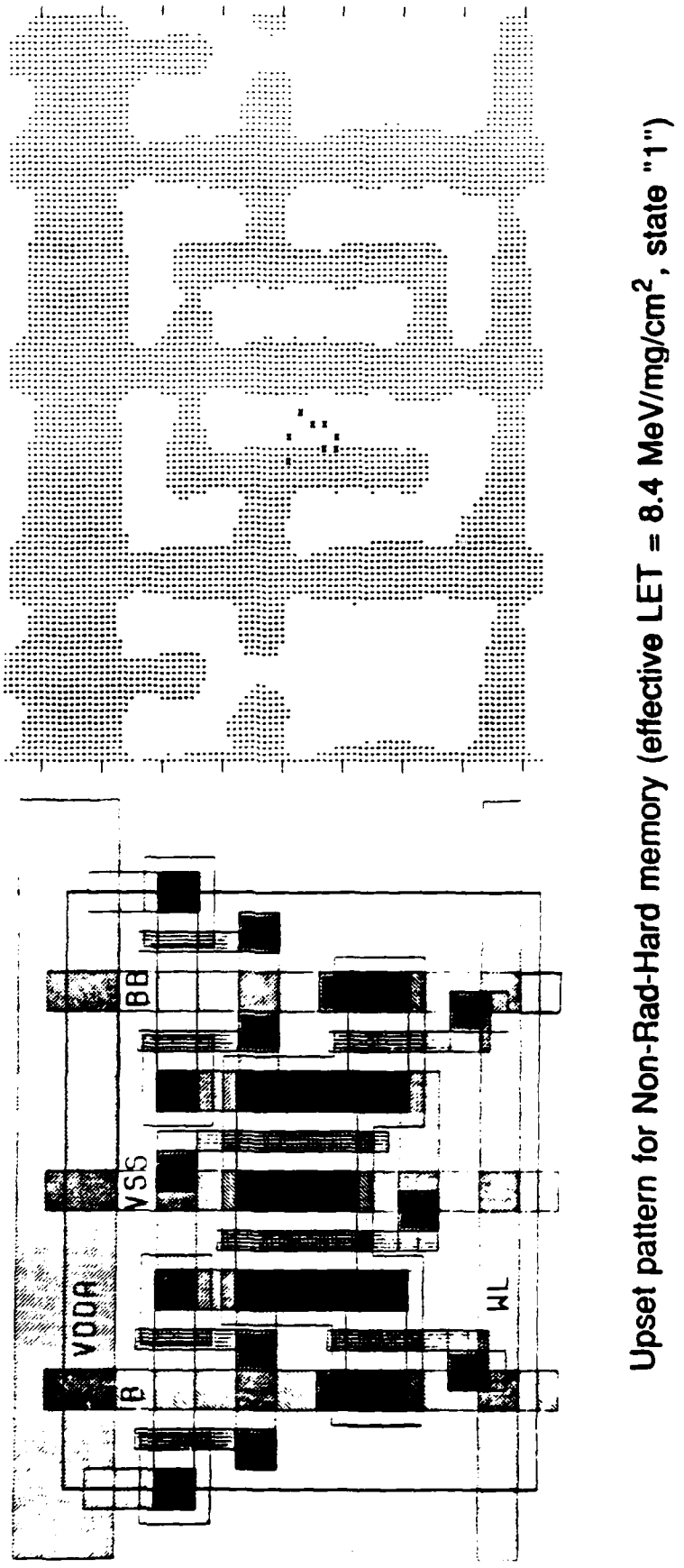


Figure 28. Upset Pattern for Standard Memory (Effective LET = 8.4 MeV/mg/cm^2, state "1")

constant, and T = temperature in degrees Kelvin. Using the above MTF expression, a MTF of about 10^8 hours was predicted for the current density of 10^5 A/cm^2 and temperature of 55°C.

The Reliability Plan for the DARPA III Pilot Line Program was submitted and approved by DARPA. In this reliability procedure, one circuit from each family of circuits (logic and memory) will be subjected to high temperature operating bias (HTOB) aging at three different temperatures. Testing will allow the determination of the failure distribution, failure mode activation energy, and median life time. The reliability tests will follow the guidelines of MIL-STD-883C, Method 1016, where appropriate. In addition, the reliability evaluation module (REM) will be used to evaluate circuit elements and structures, and identify potential reliability problem areas. The results from all the reliability tests will be fed back to the design, materials, and processing areas so that corrective action can be taken, if necessary.

APPENDIX A

Industry Survey of High Speed Packages

Revised September, 1988

(K. J. Brady and R. S. Moyer)

Introduction

The industry survey of high speed packages presented in the June 2, 1988 Semi-annual Technical Report has been reproduced for this technical report with some modifications. Two sets of drawings have been added to the survey. Manufacturer's data sheets and/or drawings describing the packages listed in Tables A-1 and A-2 have been included at the end of this survey.

The contract Statement of Work says "Contractor shall survey the industry for appropriate high speed packages with Input/Output (I/O) ranging from 20 pins to 230 pins. The survey shall be fully documented in contract Semi-Annual Technical Reports." We shall interpret "appropriate high speed" term as meaning appropriate to the chips being designed for the contract, i.e. for clock speed of 200 MHz.

There are hundreds of packages available in the marketplace, but very few have the necessary combination of high-speed capability and high I/O count. Typically, a high-speed chip and its package are designed serially, with the package designed to the specific geometric and electrical requirements of the chip and also the system requirements of the circuit.

In contrast to the ideal situation described above, where the package is custom-designed to the chip and its application, this contract requires that we locate suitable high–speed packages in the marketplace in which the demonstration circuits are to be delivered. Inherent in such a strategy is the need for minimizing the performance loss possibly associated with non-custom packages.

To find the optimum commercial packages, we will consider only those packages whose characteristics are consistent with high-speed operation, and will organize the package data of this survey into areas of concern for high speed operation. A candidate package for one of our deliverable circuits can thus be analyzed for suitability by determining the performance risk associated with each area of concern listed. An overview of the areas of concern is shown in Figure A-1.

We have divided the packaged circuit into five areas of concern:

I. **Chip-to-Cavity Match** The chip obviously has to fit into the cavity, but if the cavity is too large, there is an inductance penalty in the overly-long wire bonds required.

II. **Electrical Characteristics of the Package Body** The signal rise and fall times for the circuits in the contract typically correspond to bandwidths of ~1.3 GHz, so the package must be able to transmit these signals out to the external leads at these frequences (see Figure A-2). Typically the package body should incorporate ground planes, controlled impedance signal lines, and interspersed ground and signal lines to prevent crosstalk. The performance degradation of candidate packages which don't have these design features will have to be determined on a case-by-case basis for use in the contract. Additionally, the ability to connect by-pass capacitors and terminating resistors to the package I/Os is useful for minimizing noise.

III. **External Connection Geometry** Generally, packages for IC chips fall into two broad families, through-hole mount and surface mount. The through-hole family contains the DIPs and the pin grid arrays, (PGAs). The surface mount family contains Small Outline Integrated Circuits (SOICs), chip carriers and flatpacks. Examples of these package

types are shown in Figures A-3 - A-12. The through-hole mount package pins present large discontinuities where the package pin meets the board. This large discontinuity limits the use of these packages to applications to bandwidths below 500 MHz, less than half the required bandwidth for use in this contract work.

In the surface mount family the SOIC is a molded plastic package not well suited for high frequency applications. The chip carriers and the flatpacks are the package styles best suited for high frequency applications. The flatpacks offer the least discontinuity at the package/board interface and therefore is the style most used.

IV. **Thermal Characteristics** High-speed in ICs is often associated with more power dissipation than comparable circuits operating at lower speeds, and the heat must be removed to maintain junction temperatures at low enough levels consistent with noise margins and reliability.

V. **Associated Components** All else being equal, a package system consisting of test fixturing, burn-in sockets and carriers is preferred. This aspect is often overlooked, but the best package in the world has to be connected somehow to a test system for evaluation. These system components are often as expensive and time consuming to design and make as the package itself.

The relative importance factors affecting package choice for a give chip are shown schematically in Figure A-13.

THE PACKAGE SURVEY

Several manufacturers offer open-tooled packages with controlled impedance signal lines for high frequency applications. The manufacturers and the packages they offer are listed in Table A-1. Manufacturer's data sheets and/or drawings of these packages are given in the attached figures. The pin counts offered cover the range from 20 to 164 with signal line counts from 8 to 148. Listed at the bottom of Table A-1 are several package from Mini Systems Inc. (MSI), these packages do not have controlled impedance signal lines, but these packages have been tested and found to be useful at frequencies up to 2 GHz.

Two points are obvious from the entries in Table A-1. First, the packages at the top of the table have been designed to have a characteristic impedance, Zo=50Ω. The second point is that the entries in the table do not cover the high end of the pin count range. For example, the Casino Test Chip has 177 signal lines, therefore, none of the packages listed could accommodate this chip.

Devices designed to operate with 75Ω characteristic impedance signal lines would dissipate less power. Consequently, the three manufacturers listed at the top of the Table A-1 were asked about the possibility of designing packages with 75Ω characteristic impedance transmission lines. The two ceramic manufacturers, Interamics and TriQuint answered that they felt that such high impedance packages would not be manufacturable. The reason for this is the high dielectric constant of the alumina ceramic, E_r = 9.6, and the relation that governs the characteristic impedance Zo of a transmission line:

$$Zo = \sqrt{\frac{L}{C}} = \frac{[\text{Geometric Factors}]}{\sqrt{E_r}}$$

where L = inductance per unit length, C = the capacitance per unit length, and E_r = the dielectric constant. To produce a package with 75Ω characteristics impedance signal lines would require pushing the geometric factors to values which are impractical for manufacture. Only Rogers-Microtic using polymide with $E_r \leq 3.8$ would attempt to fabricate packages with 75Ω impedance signal lines. Some samples of packages with 75Ω signal lines have been ordered from Rogers-Microtic but have not yet been delivered and are in fact six months late from the promised delivery date, indicating some difficulty in achieving the required 75Ω characteristics.

Since packages with controlled impedance signal lines are not available with sufficient signal line count, the second option is to keep the length of these signal lines to a minimum. The length of these lines should be less then $\frac{\lambda}{4}$ where λ is the signal wavelength. An estimate of the signal wavelength can be obtained from the signal rise time (see Figure A-2). The equivalent frequency is approximately 1.3 GHz and this leads to a signal wavelength of approximately 7.5 cm; thus $\frac{\lambda}{4} \approx 1.9$ cm. Therefore, the second choice in selecting packages for this application is to choose those packages with signal line lengths less than 1.9 cm.

The viability of this second option is demonstrated by the experience with the MSI packages listed at the bottom of Table A-1. These packages do not have controlled impedance signal lines, yet they have been shown to be useful up to frequencies of 2 GHz. The reason for this is the packages are very small, and the length of the signal lines is very small compared to the signal wavelength.

There are two types of packages that have pin counts that cover the high end of the required range, the pin grid arrays (PGA's) and the fine pitch leaded chip carriers or flatpacks. The PGA's are through hole mount packages and as noted earlier are not used for high frequency applications because of the severe impedance discontinuity at the pin/board interface. The other type of package, the leaded flatpack, is the choice for high frequency applications. All of the entries in Table A-1 are leaded flatpacks, whether standard lead pitch, .050", or fine pitch with lead center ≤ .050".

Table A-2 is a list of available production tooled leaded flatpacks with pincounts above the 148 signal lines of the packages listed in Table A-1. Manufacturer's drawings and/or data sheets are presented in the attached figures; the packages listed in table A-2. These packages do not have dedicated ground and power lines so all lines are potentially available for signals. All the lines on these packages satisfy the line length requirement noted above. The converse of the fact that all lines are potential signal lines is the fact that these packages do not have built-in ground and power planes. The lack of these built-in planes will mean significantly increased cross-talk on the signal lines and significantly increased inductive noise on the DC lines. The obvious way to reduce these problems is to intersperse among the signal lines as many as possible ground and power lines. The ideal would be a ground-signal-ground line arrangement. Table A-2 lists the body size, the lead pitch and the cavity size for the flatpack packages. The packages listed are all fine pitch, with lead pitch of .020" or .025". Also listed is the information on the availability of carriers and (low frequency) sockets for the packages.

Carriers and sockets are considered **necessary** support elements to the chip packaging operation; **if they do not exist, they will have to be developed.** It is not possible to deliver devices in fine pitch flatpacks without carriers and sockets.

Listed at the bottom of Table A-2 is a 256 I/O flatpack designed by AT&T for the EMSP project. AT&T has given permission to use this package and its supporting carriers and sockets in the DARPA project. The package has been production tooled and parts are on hand. The supporting carriers and sockets have been developed and will be available starting in May, 1988.

In addition to the availability of the support elements the EMSP has two electrical advantages. The first is that the package does have a built-in ground plane and although it is not ideally located, this ground plane still offers significant reduction in signal cross-talk. The second is that with the highest available I/O count the package offers the best opportunity of distributing DC lines among the signals.

THE FOLLOWING SECTION DESCRIBES HOW THE RESULT OF THE IN HIGH SPEED REQUIREMENTS TO SELECT PACKAGES FOR THE CONTRACT.

RECOMMENDATIONS

The 24 signal, 44 total I/O package from TriQuint was selected for use with the PT-1 chips. This is a true high frequency package, designed with 50Ω signal lines and provision for mounting bypass capacitors on the package. It is recommended that this package be used for the final 4K SRAM. The package is ceramic can be hermetically sealed. A photograph of this package is shown in Figure A-14. The body of the package is .650" sq. with leads on .050" pitch. Carriers are not necessary for packages with this pitch. Low frequency sockets are available for this package. A high frequency test fixture is also commercially available to fit this package. Some preliminary tests have shown that this test fixture performs well to frequencies beyond 1GHz, certainly sufficient for the present application.

Another important feature of this package is that it is designed to accommodate high power chips. The die attach substrate is a copper/tungsten composite that is coexpansive with the ceramic body but has a thermal conductivity an order of magnitude higher than ceramic. This high conductivity die mount is not the total solution to the thermal management problem for a high power chip but it is an important contribution to the solution.

The 64 signal, 88 total I/O package from Interamics was selected for use with the PT-2 logic chips. Again, this is a true high frequency package with 50Ω signal lines, some built in bypass capacitance and the high thermal conductivity die attach substrate. This package is recommended for use with any of the logic chip deliverables. A photograph of this package is shown in Figure A-15. This package is also ceramic with provision for a hermetic seal. The package body is .500" sq. with 23 leads per side, at .020" pitch. (The two leads that surround each of the four corners are tied together, hence the designation 88 rather than 92 total I/O.) This is a fine pitch package, but the carriers and sockets are not available, neither are high speed test fixtures. These support elements will have to be developed.

The 256 I/O fine pitch leaded flatpack designed by AT&T for the EMSP project appears to be the best available package for the high pin count logic devices. A photograph of this package is shown in Figure A-16. This package is not ideal but it does have several advantages,

namely a built-in ground plane, spare I/O for signal isolation, and available carriers and sockets. The principal drawback to this package is that the die cavity (.560"sq.) is too large for the expected size of the Casino Test Chip, .320"sq. This same problem exists to a greater or lesser extent for all of the high pin count packages however. The high frequency test fixtures for this package will have to be developed, but this same development would be required for any of the high pin count packages. The 256 I/O package does not have a high thermal conductivity die attach substrate, but again neither do any of the other high pin count packages. This adds an important resistance in the heat flow path but it doesn't preclude a solution to the thermal management problem.

A request for approval to use the 256 I/O EMSP will be submitted to the COTR.

TABLE A-1

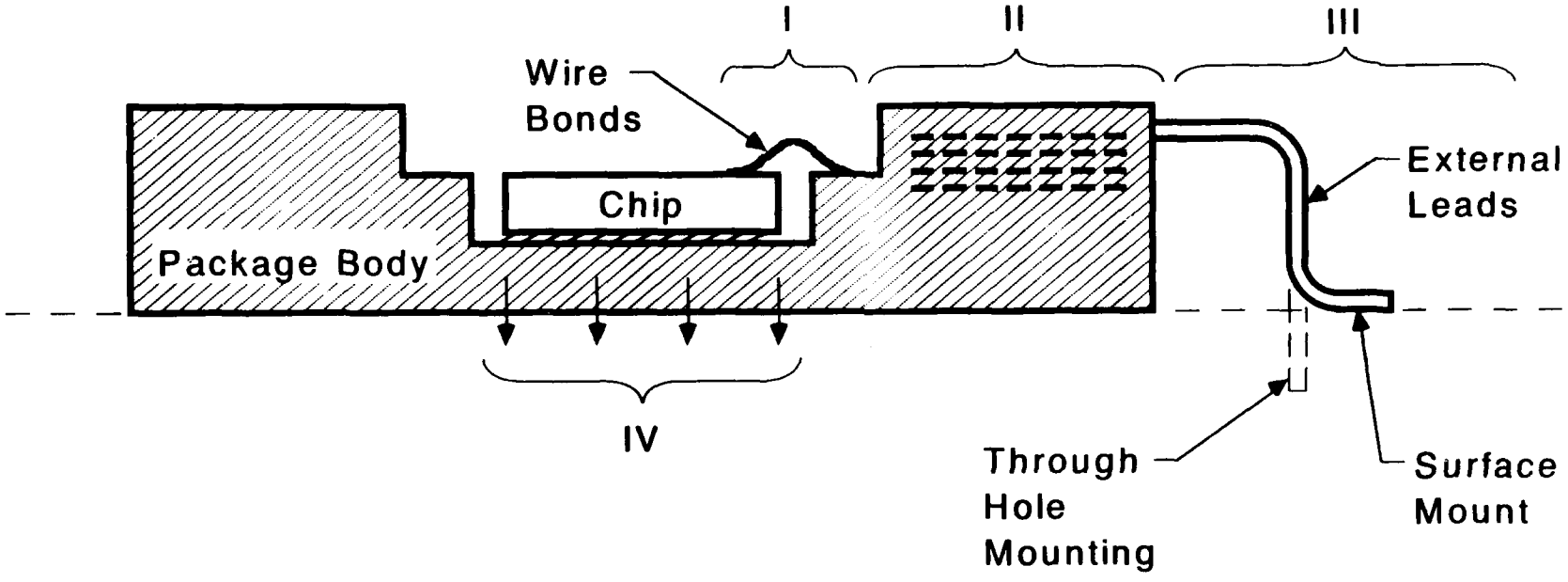
Packages with Controlled Impedance (Zo = 50Ω) Signal Lines

VENDOR	I/O COUNT (SIGNAL/TOTAL)	PACKAGE BODY MATERIAL	CAVITY SIZE (in)	COMMENTS
INTERAMICS	28/32	ALUMINA	.190X.250	
	64/88	"	.250X.250	MAYO DESIGN
TRIQUINT	8/20	ALUMINA	.060X.060 (CHIP)	NO CAVITY, PERFORMANCE VERIFIED TO 18GHz
	24/44	"	.130X.130	PROVISION FOR MOUNTING BYPASS CAPACITORS.
	64/132	"	.210x.210	PROVISION FOR MOUNTING BYPASS CAPACITORS.
ROGERS - MICROTEC	64/88	POLYMIDE	.250X.250	MAYO DESIGN
	116/132	"	.400X.400	PROVISION FOR MOUNTING BYPASS CAPACITORS.
	148/164	"	.400X.400	PROVISION FOR MOUNTING BYPASS CAPACITORS.
Additional Packages Usable in High Frequency Applications				
MSI	20/20	ALUMINA	.140X.140	PACKAGE BODY .270"SQ.
	32/32	"	.265X.265	" " "
	64/64	"	.360X.360	PACKAGE BODY .640"SQ.
	84/84	"	.300X.300	" " "

TABLE A-2

High I/O Count Leaded Flatpacks

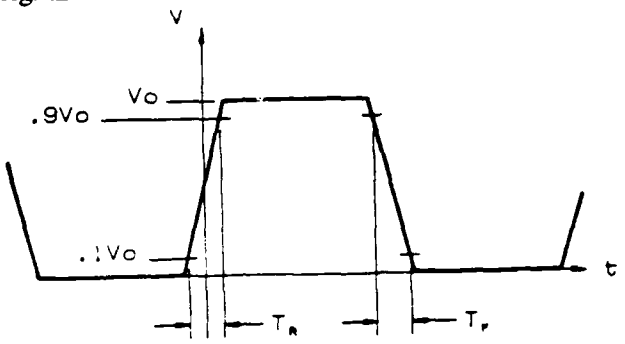
I/O #	Manufacturer	I/O Pitch in.	Body Size in. (SQ)	Cavity Size in.	Carrier/Burn-In Socket	Comments
152	NTK	.020	.840	.380x.380	YES	Open Tooled, No Ground or Power Planes
172	NTK	.020	.940	.380x.380	YES	
172	KYOCERA	.025	1.150	.380x.380	NO	
196	KYOCERA	.025	1.350	.410x.410	NO	
256	NTK	.020	1.380	.540x.550	YES	
256	KYOCERA	.020	1.480	.500x.500	NO	
256	NTK	.020	1.450	.560X.560	YES	AT&T design, Ground and Power Planes



Cross Section Of Chip Assembly, Showing Critical Areas For High-Speed Suitability. (Lid Omitted For Clarity)

Figure A-1. Cross Section of Chip Assembly

To obtain a signal frequency from a signal with a known signal rise time T_r and signal fall time T_f, one compares the signal



to a sine wave with the same amplitude and the unknown frequency f,

$$V(t) = \frac{Vo}{2} [1 + \sin 2 \Pi ft]$$

For simplicity assume $T_r = T_f$, then equating the sine wave value to the signal value at $t=T_r/2$ yields

$$.9Vo = \frac{Vo}{2} [1 + \sin \Pi fT_r]$$

which has the solution

$$f = \frac{\sin^{-1}(.80)}{\Pi T_r} \approx \frac{.295}{T_r}$$

For a signal with a rise time T_r = 225 ps, the frequency is

$$f \approx 1.3 \text{ GHZ}$$

Then, from the wavelength/frequency relationship

$$\lambda f = \frac{C}{\sqrt{E_r}}$$

where λ is the wavelength, C is the speed of light and E_r is the relative dielectric constant for the package body material. For a ceramic package $E_r = 9.6$, then

$$\lambda = 7.4cm$$

Figure A-2. The Calculation of the Signal Frequency and Wavelength

The calculation of the signal frequency and wavelength from the signal rise time

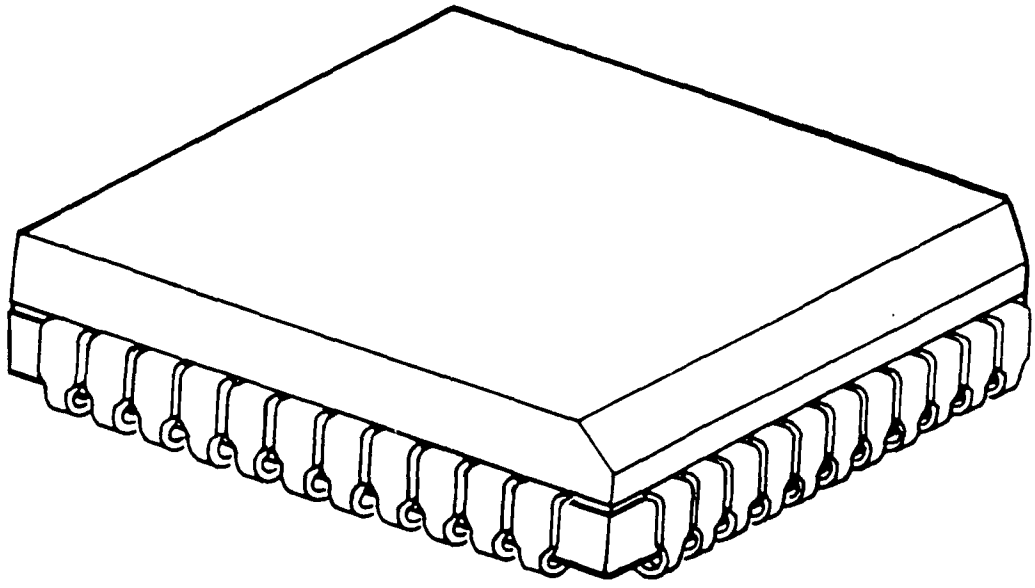


Figure A-3: Post Molded Plastic Chip Carrier

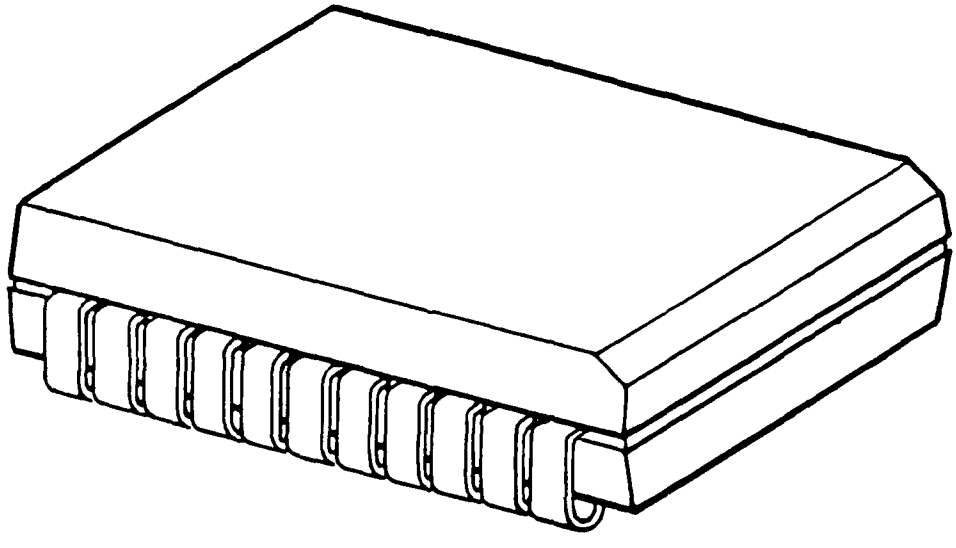


Figure A-4: SOJ (Small Outline J Lead)

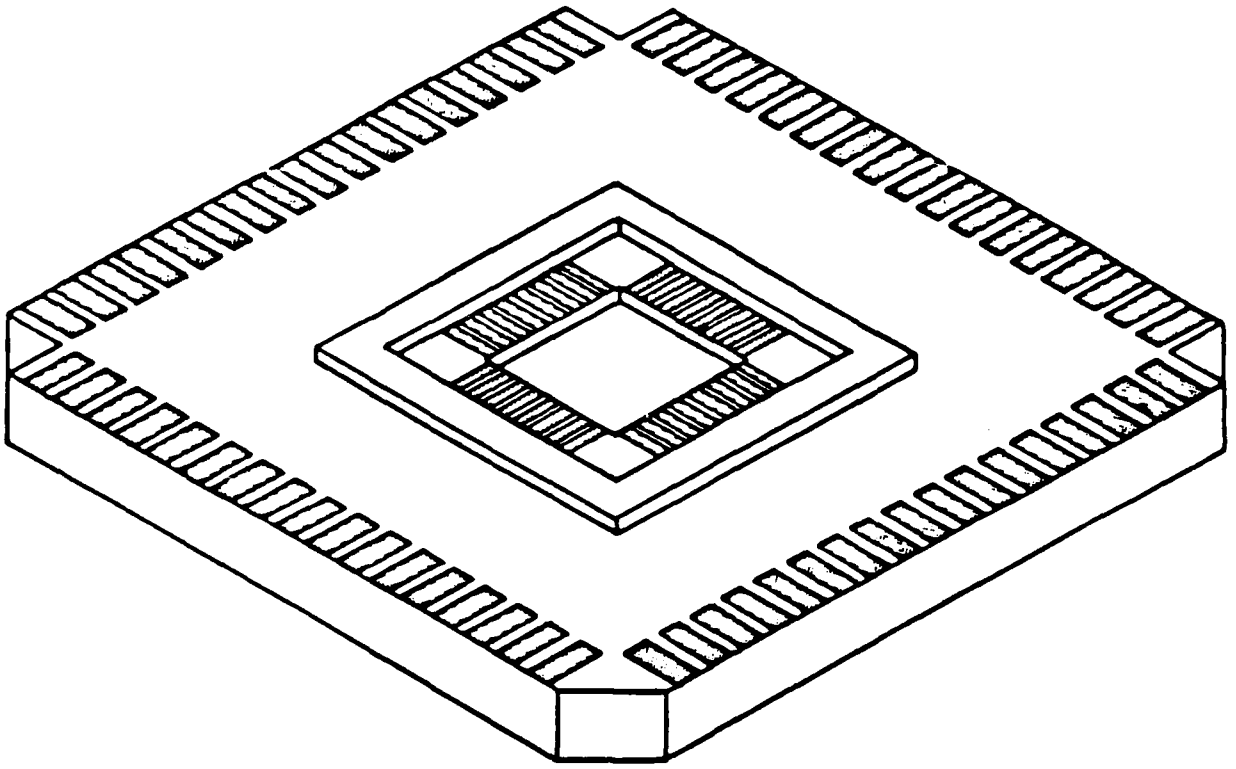


Figure A-5: Leadless Ceramic Chip Carrier

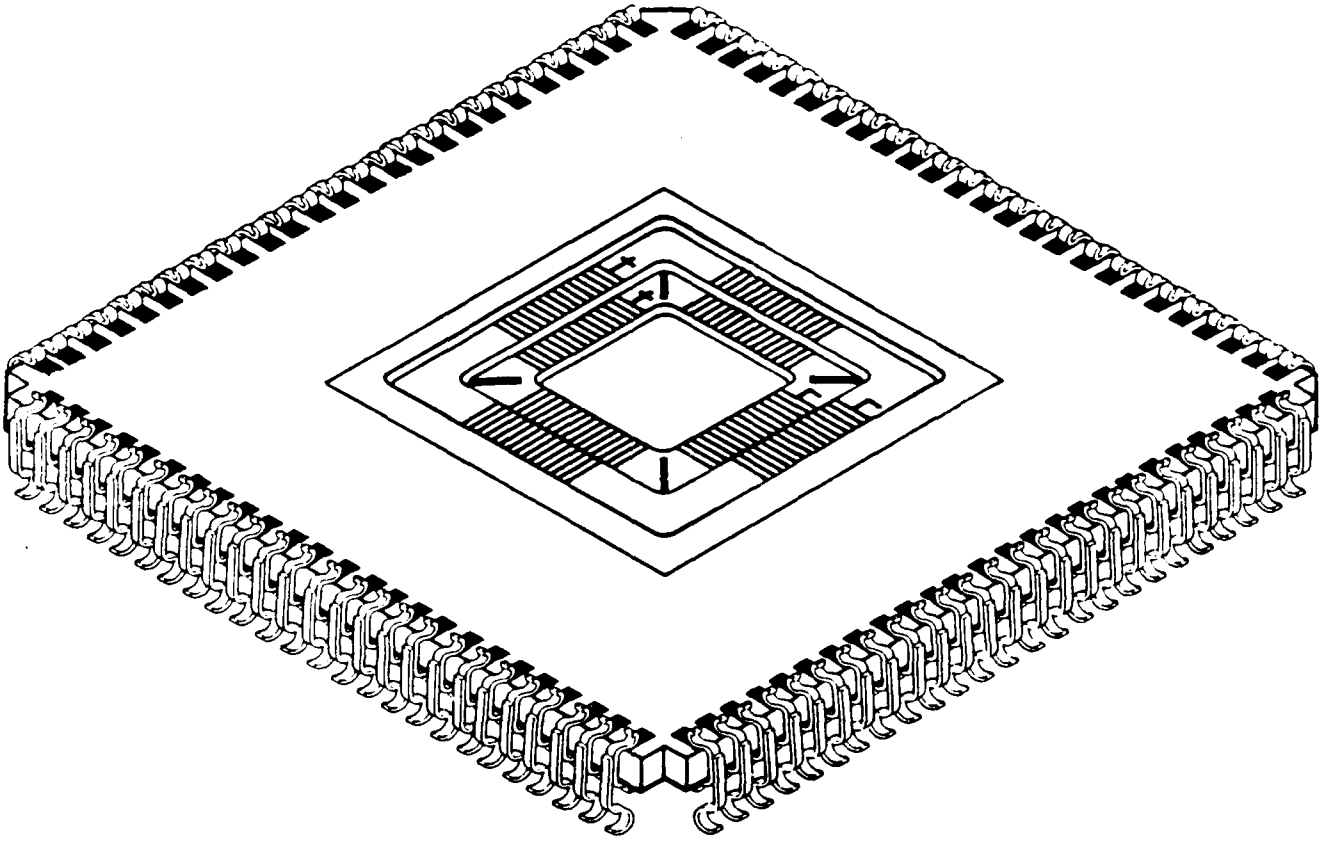


Figure A-6: Leaded Ceramic Chip Carrier

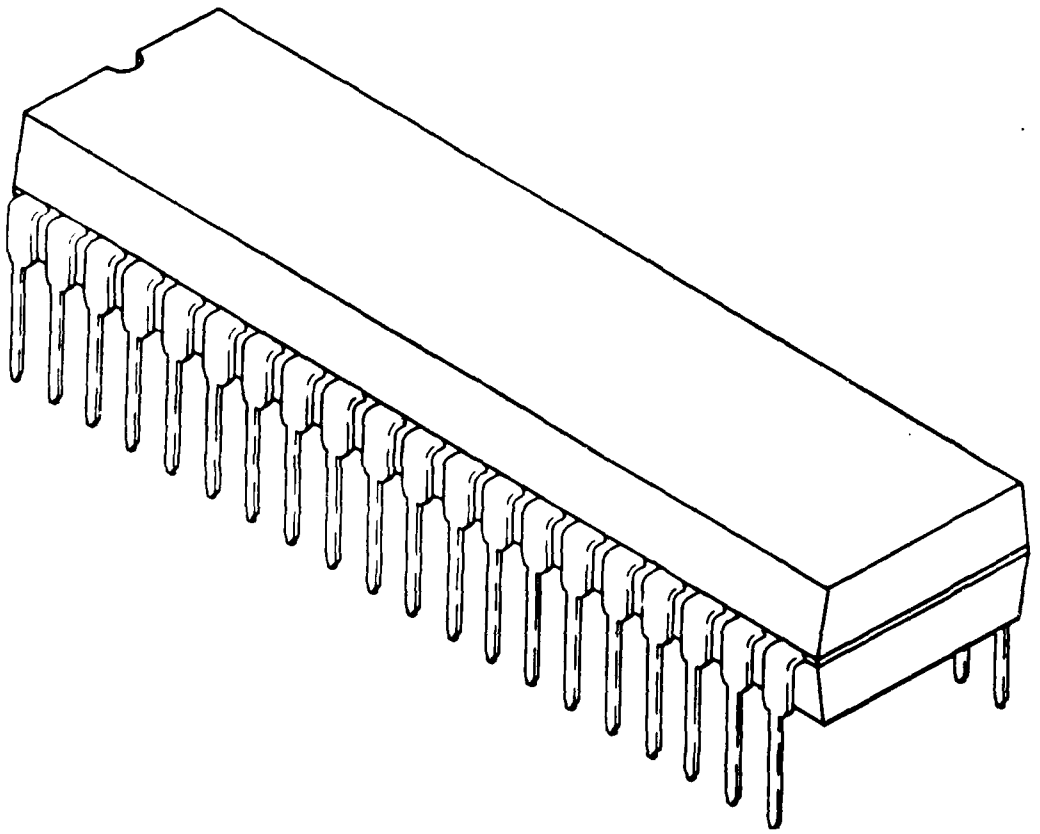


Figure A-7: Post Molded Plastic Dip

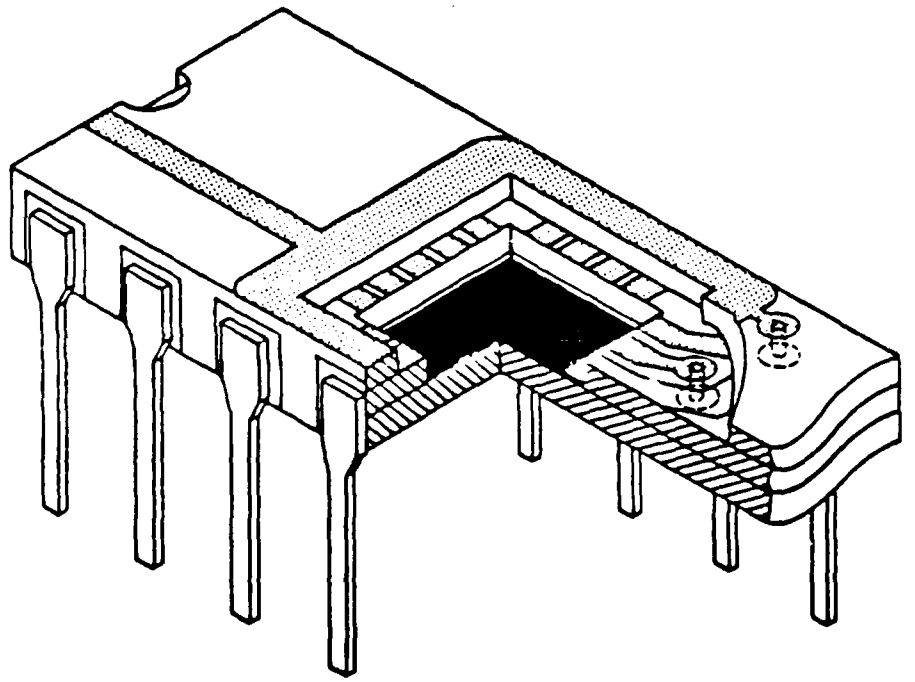


Figure A-8: Ceramic Dip

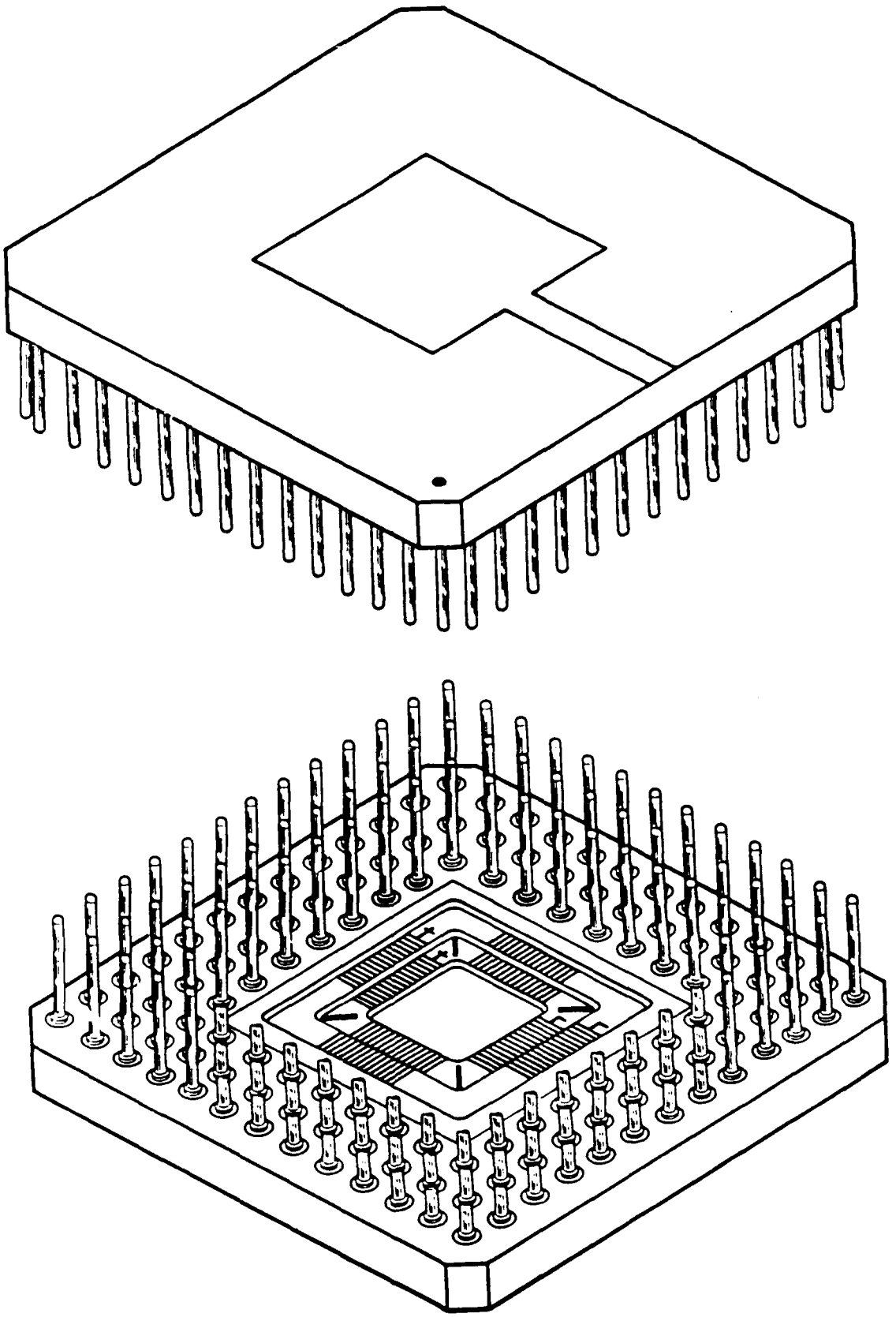
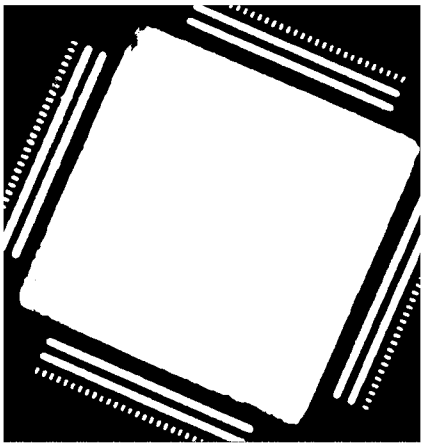
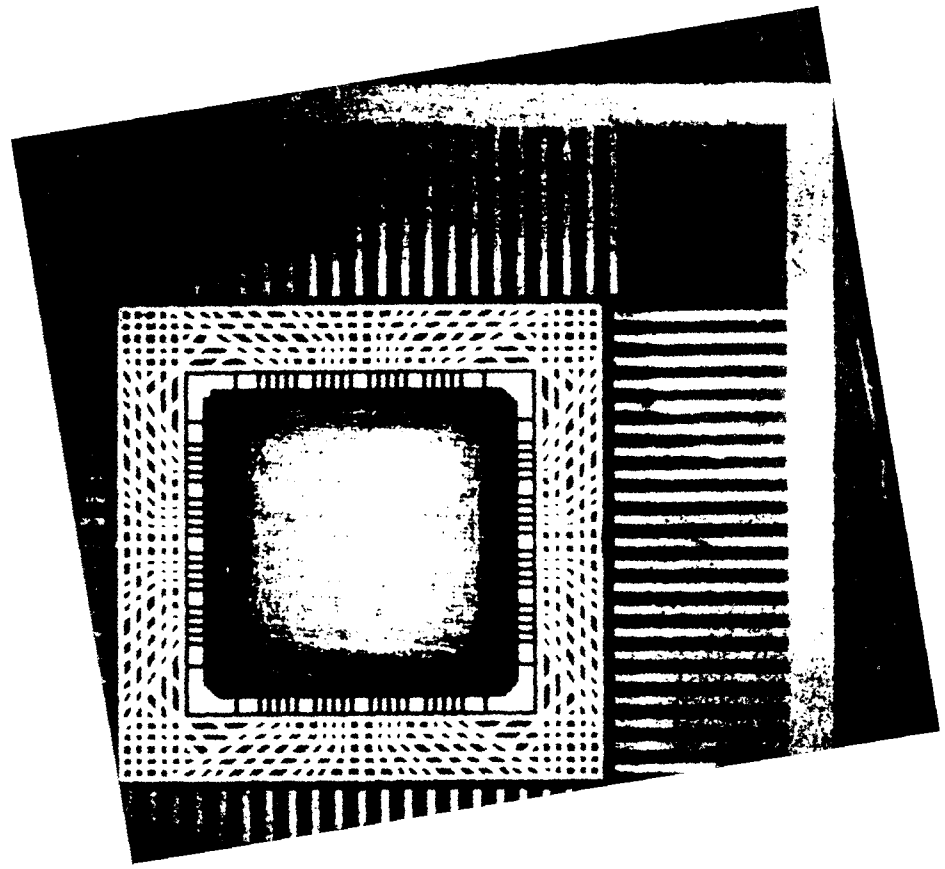
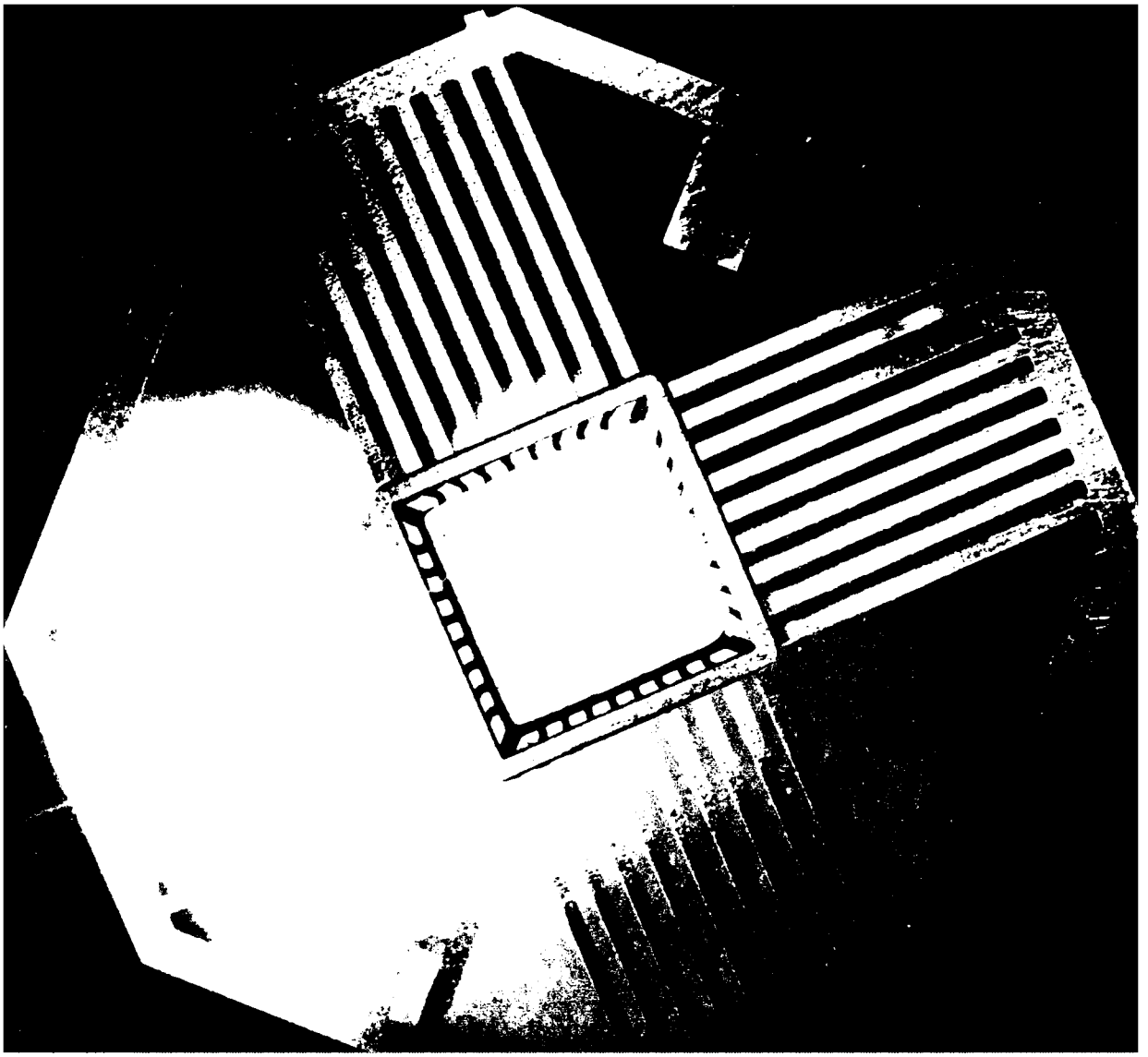


Figure A-9: Ceramic Pin Grid Array







HIGH-SPEED PACKAGE SELECTION PROCESS

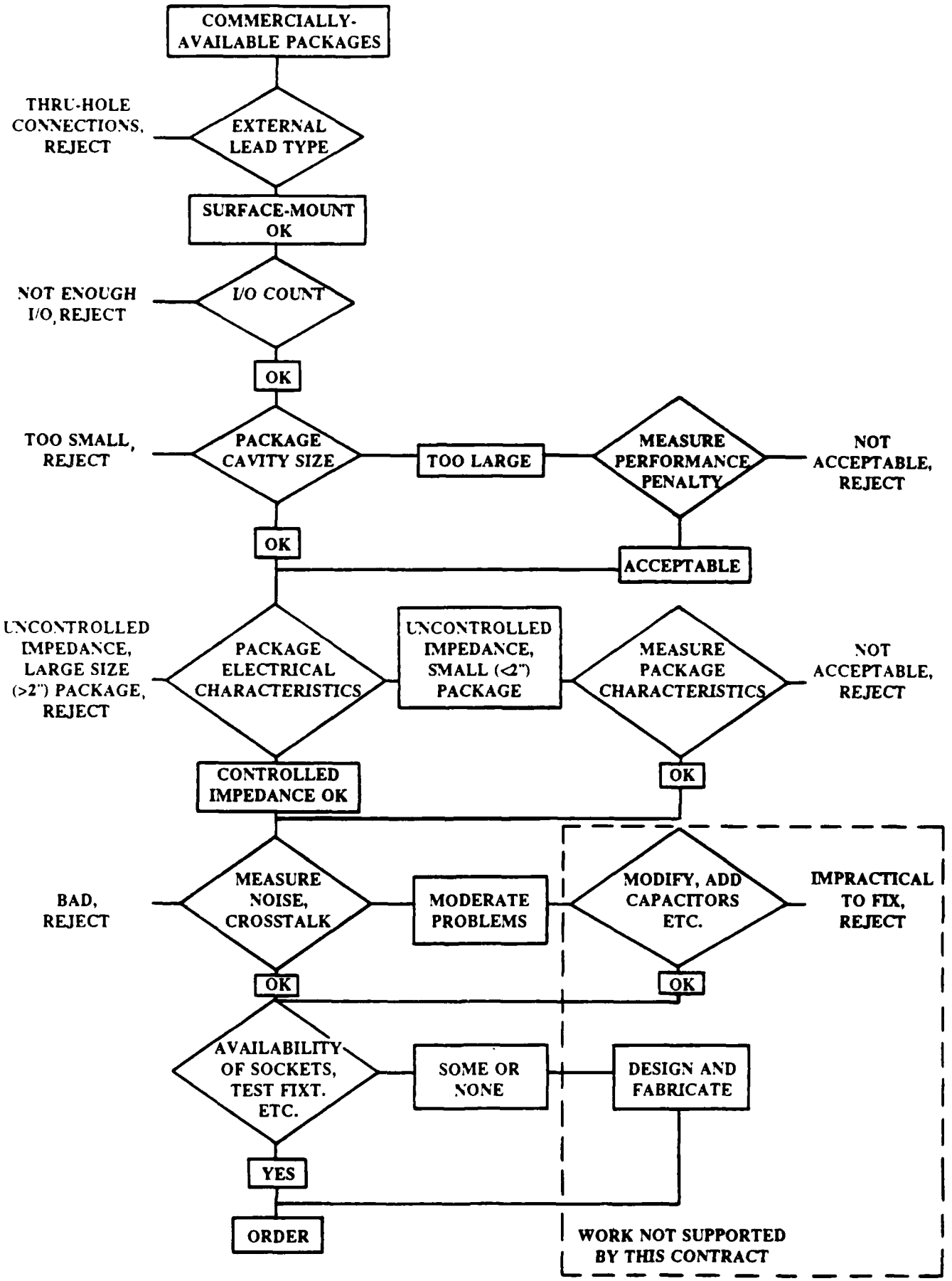
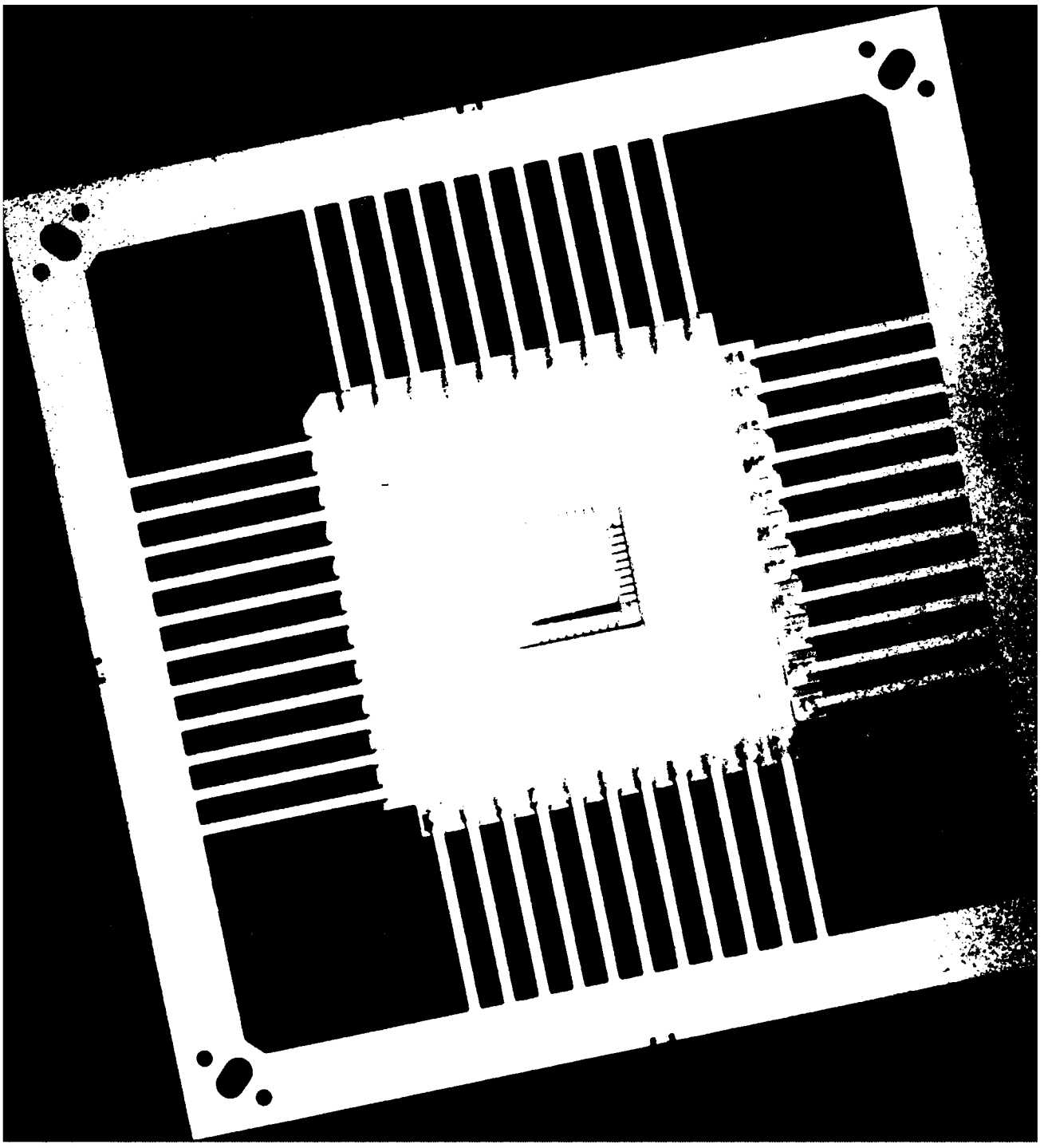
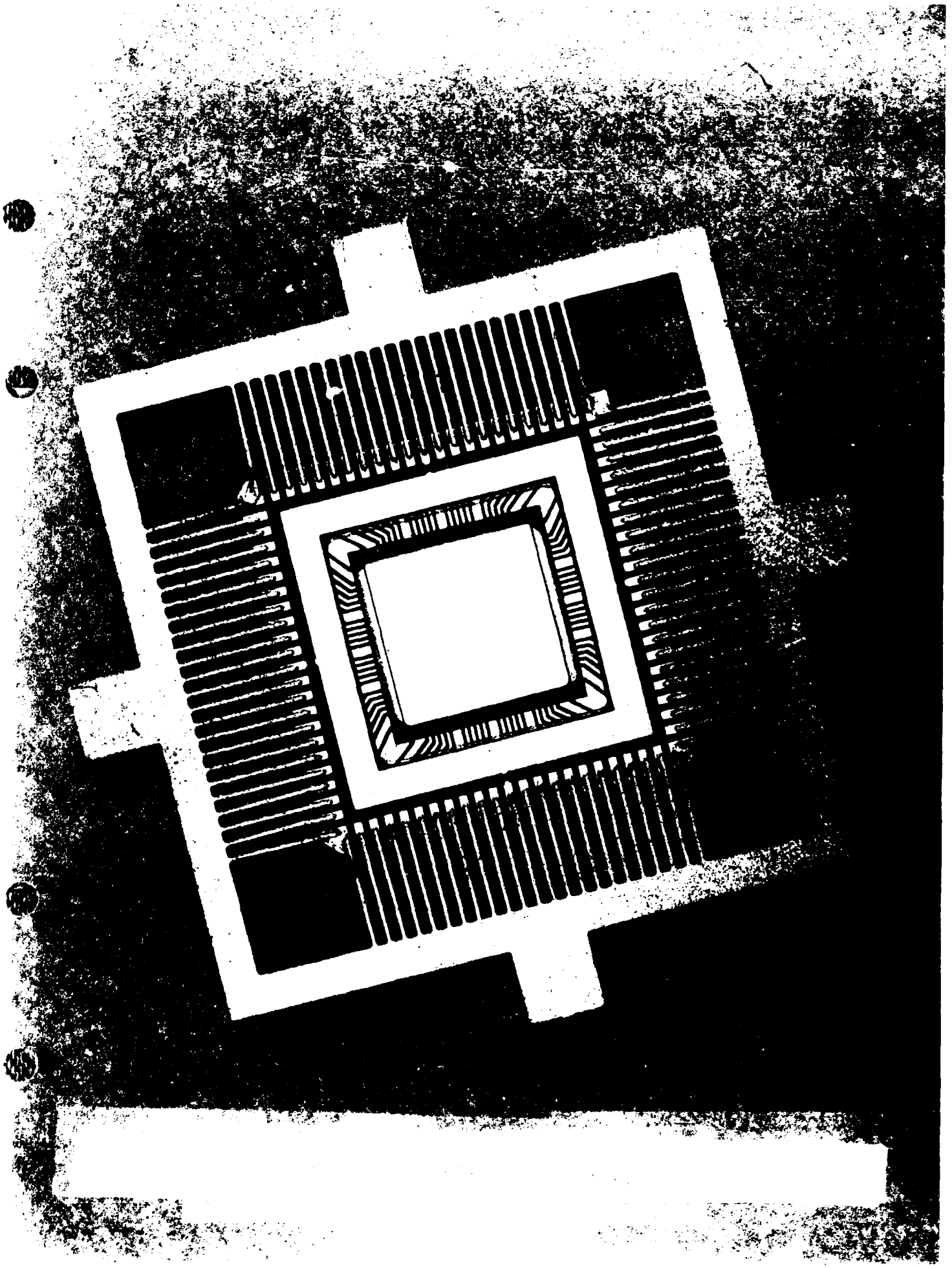
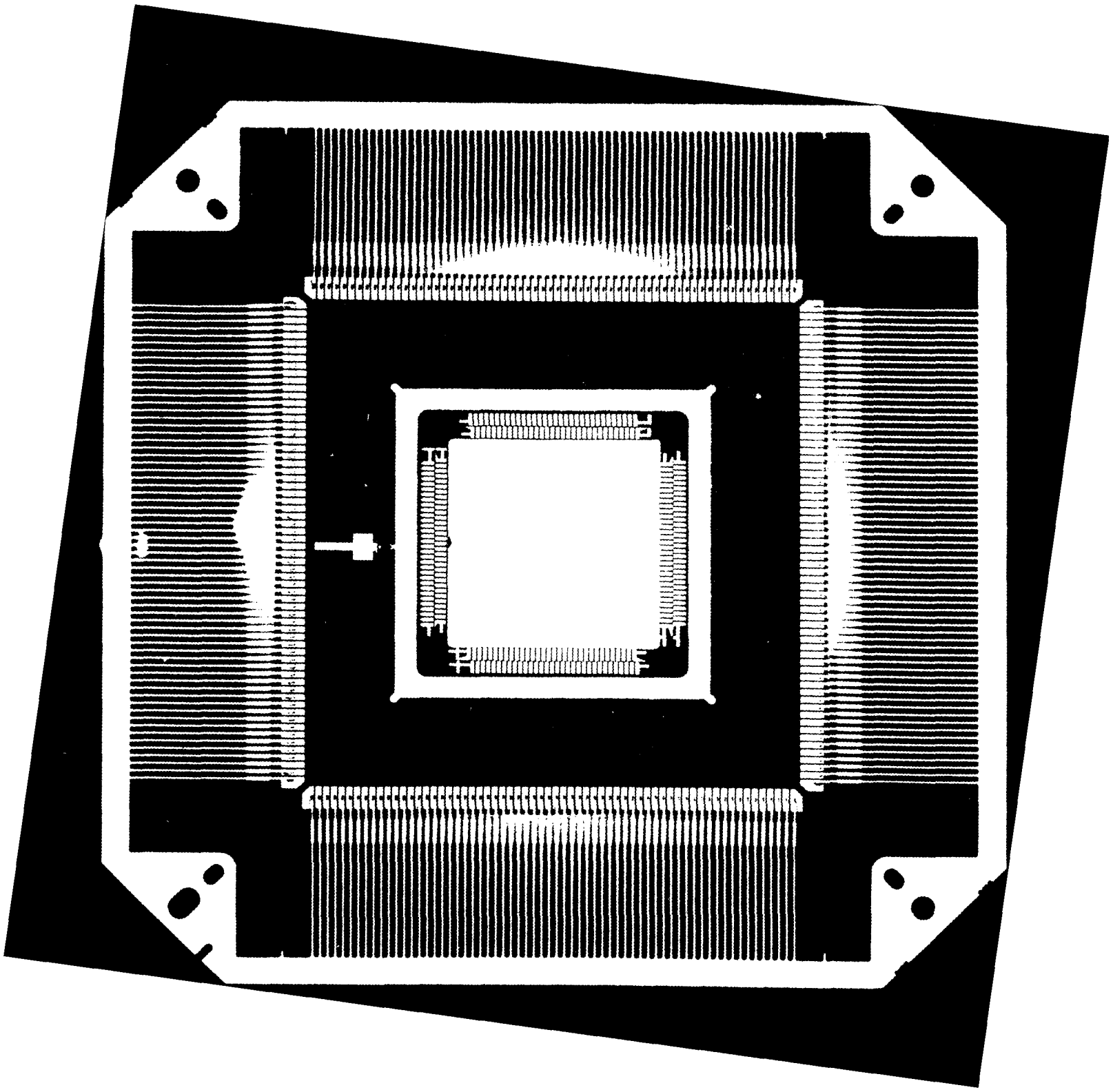


Figure A-13. High Speed Package Selection Process







Drawings for Packages

Described in Table A-1

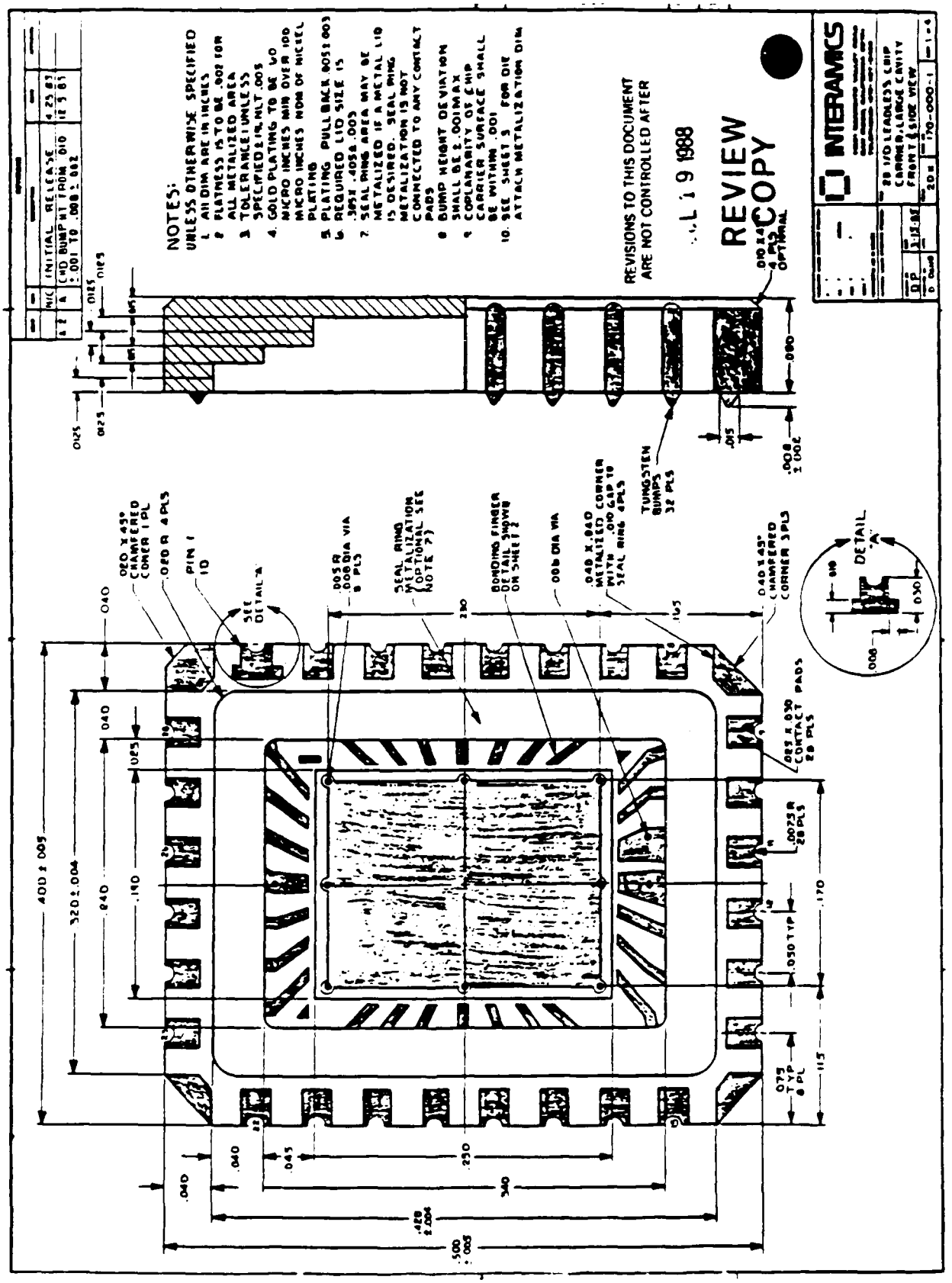


Figure A-17. Interamics 28/32 Leadless Package

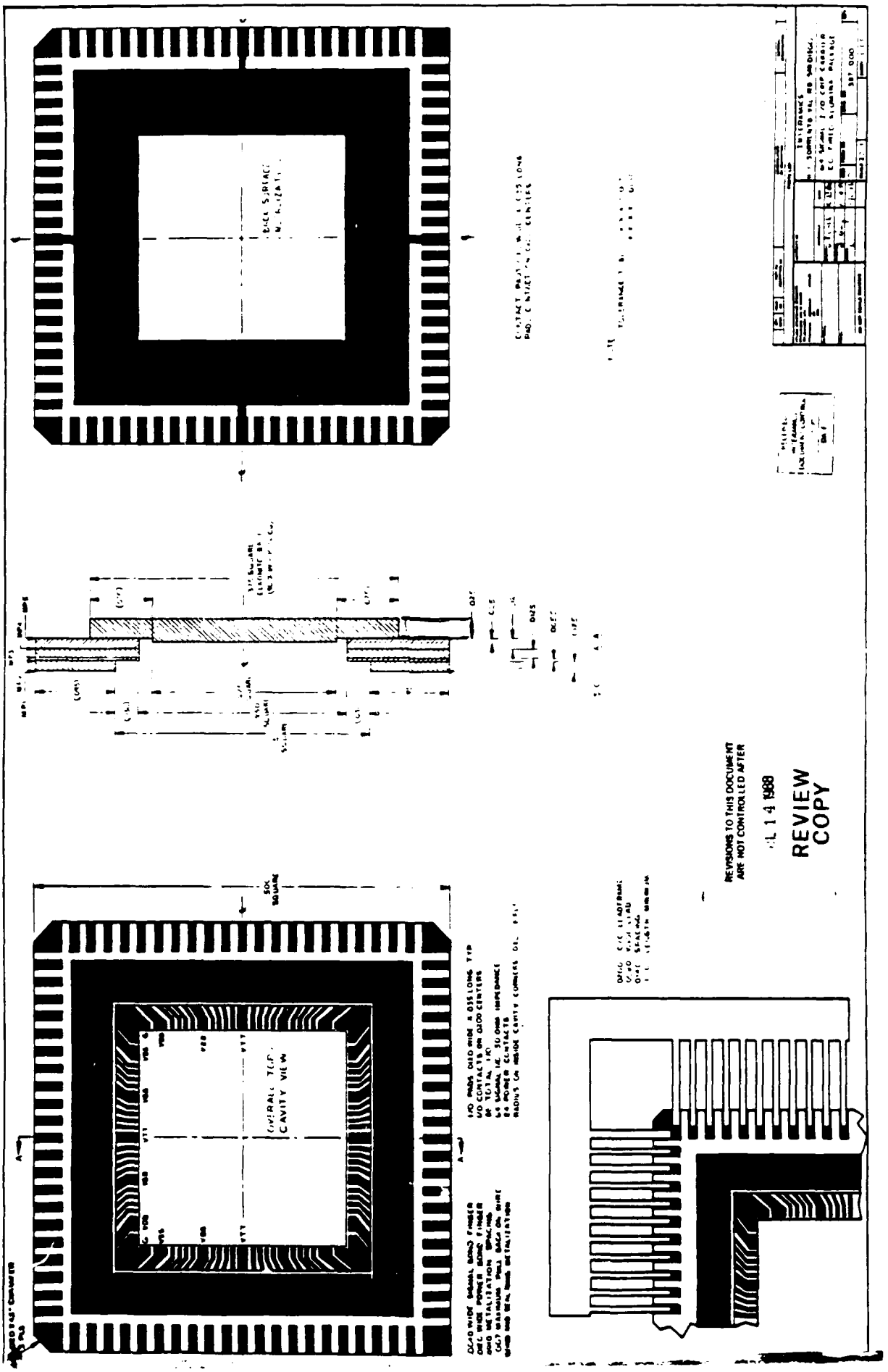
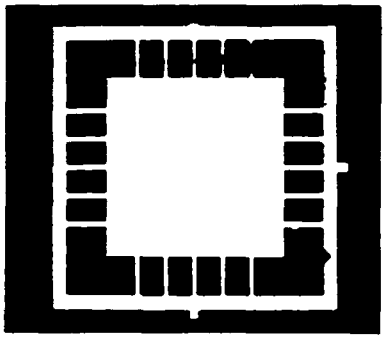
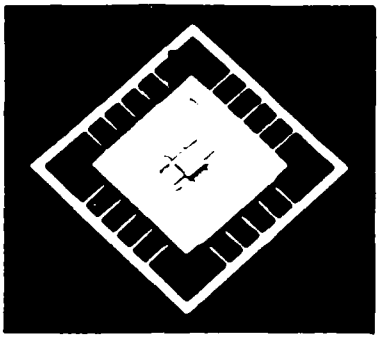


Figure A-18. Interamics 64/88 Leaded Package

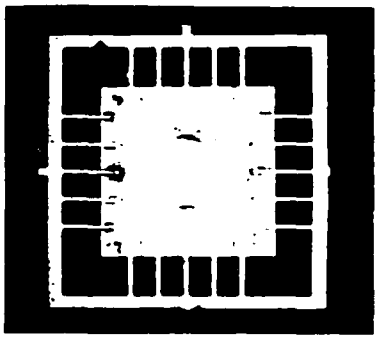
TEKPAC:™ HERMETIC MMIC PACKAGE PRODUCT LINE



TPAX142 (top view)



Typical Application used in Micro-S product line. TriQuint Semiconductor, Inc



TPAX142 (bottom view)

TEKPAC™ Hermetic MMIC Packages

- Multiple RF signal lines from motherboard to chip
- 10^{-8} atm cc/sec hermeticity
- Direct-contact heatsinking

The TPAX Series MMIC package represents a new benchmark for low-cost surface-mountable and hermetically sealable microelectronic packages designed for Monolithic Microwave Integrated Circuits (MMICs).

The TPAX Series is a first in a series of low-cost 12 GHz performance MMIC packages. Thick film technology and well established fabrication techniques provide a cost-effective solution without sacrificing performance.

TPAX142 CHARACTERISTICS

	0–6 GHz	6–12 GHz
VSWR[1]	1.2:1 max	2.0:1 max
Insertion loss[1]	5 dB max	1 dB max
Isolation[2]	40 dB min	30 dB min

[1] *Measured for one signal line from leadframe to die attach pad.*

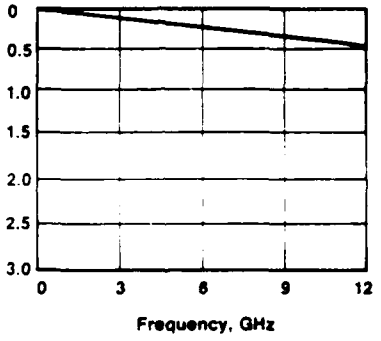
[2] *Measured for two opposite signal lines with all unconnected lines grounded.*

Environmentally tested per MIL-STD-883.

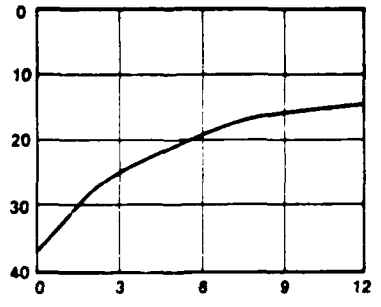
OTHER SERVICES AVAILABLE

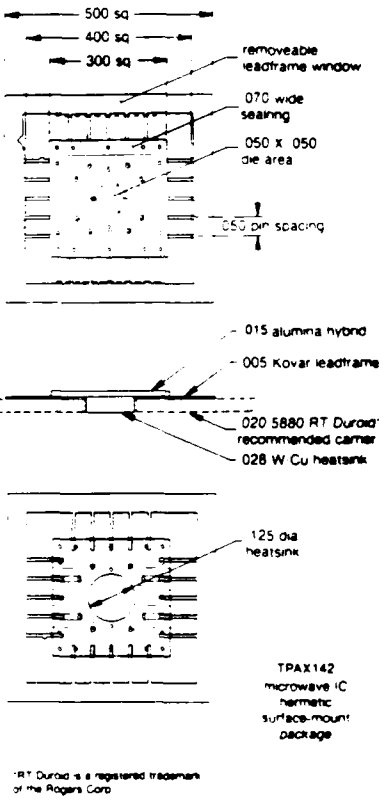
- Product technology licensing
- Custom design applications

INSERTION LOSS dB (TYPICAL)



RETURN LOSS dB (TYPICAL)





®RT Duroid is a registered trademark of the Rogers Corp.

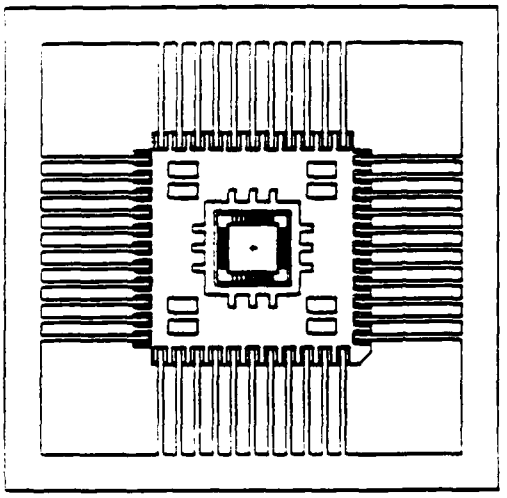
ORDERING INFORMATION

Tektronix Product	Frequency Performance	Case Size (inches)	Motherboard Recommended	Diepad Area (inches)	TEKPAC Options
TPAX142	12 GHz	3 x 3	020 5880 RT Duroid	054 x 054	Option 01—Lid perform set Option 05—Leadframe window removed

TKIT14F — Evaluation kit for the TPAX142

Tektronix
COMMITTED TO EXCELLENCE

Figure A-19. TriQuint 8/20 Leaded Package



44 LEAD HIGH SPEED CERAMIC PACKAGE

FEATURES:

- *24 High-Speed 50-Ohm Controlled Impedance Signal Lines*
- *Power Supply Decoupling via Power Planes and Optional On-Package Capacitors*
- *Multiple Power and Ground Connections*
- *Optional Metalized Seal Ring for Hermetic Sealing*

DESCRIPTION

The MLC44 package is a high-speed multilayer ceramic package developed at TriQuint to support the special requirements of very high performance ICs. The package is designed to handle clock rates up to 4GHz and fast edge speeds less than 100ps. Signals are carried on 50-Ohm controlled impedance transmission lines from the package leads to the bond pads. Excellent signal isolation is provided by the use of multiple ground lines. Capacitive power planes and decoupling capacitors minimize switching noise on the power supplies.

The package is fabricated from cofired alumina ceramic. In most applications it easily handles power dissipation of 1 Watt, and can handle 3-4 Watts with the addition of a suitable heat sink. The package is suited for surface mounting with appropriate lead bend. The package body is available with a solder seal ring around the cavity, or without for epoxy sealing.

April 21, 1988 14-0083-A

TriQuint SEMICONDUCTOR

Figure A-20. TriQuint 24/44 Leaded Package; Description

SIGNAL CONNECTIONS

The illustrations below identify package pin and die cavity bond pad connections.

Each signal bond pad connects to one package pin through a 50-Ohm controlled impedance line. All the ground bonding pads are connected together, as are all the pins labeled GND. All points labeled GND are common with all the internal ground planes and the back surface of the package. Each of the two power supplies has two pins, at opposite corners of the package which are common with two corresponding bond pads at opposite corners of the bond cavity. Both power supplies and ground are brought to pads beside the bond cavity where optional decoupling capacitors may be added.

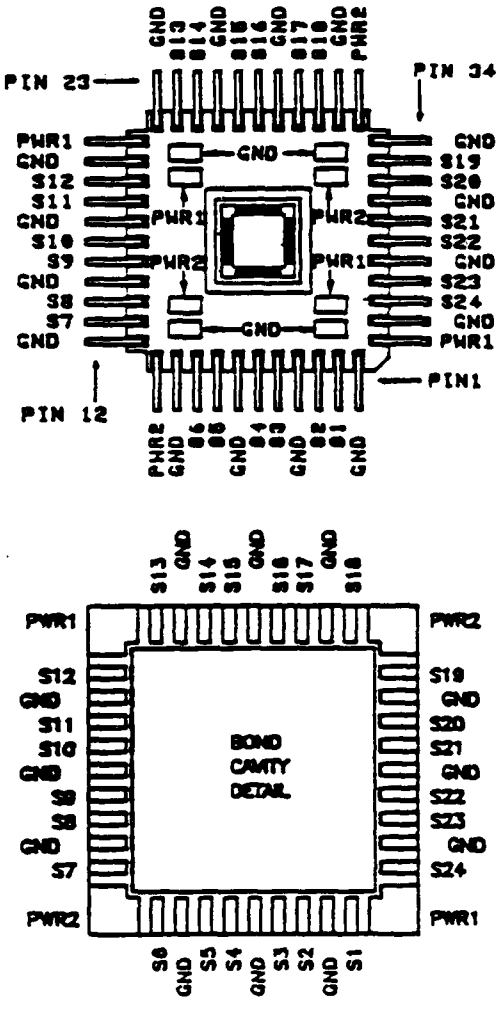
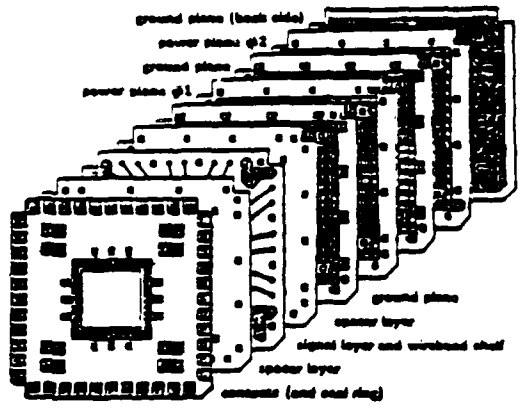


Figure A-21. TriQuint 24/44 Leaded Package; Signal Connections

PACKAGE STRUCTURE

The package is constructed of several metal layers with a layer of ceramic between each pair of metal layers. This structure gives a controlled impedance environment for the signal lines. The figure below shows a representation of the layered structure.



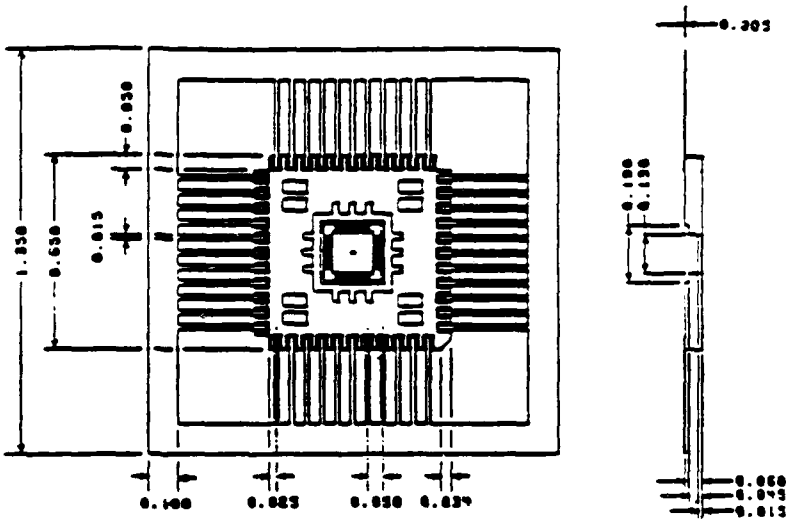
SPECIFICATIONS

Materials:	Body	Alumina Ceramic
	Leads	Kovar
	Metalization	Tungsten/Nickel/Gold
Dimensions:	Body Size	0.650 x 0.650 x 0.080 inches
	Die Cavity Size	0.130 x 0.130 inch
	Max recommended die size	0.090 x 0.090 inch
Leads:	Spacing	0.050 inch
	Lead Count	44
	Signal Leads	24
	Ground Leads	16
	Power Leads	4 (2 per supply)
Misc.	Power plane Capacitance (each supply)	150 pF
	Die-to-Case Thermal Impedance(1)	10°C/Watt

Note 1: The thermal impedance value shown is typical for a 0.080 x 0.080 die. Use thermal impedance numbers with caution; operating temperature is a complex function of die size, circuit layout, and other factors.

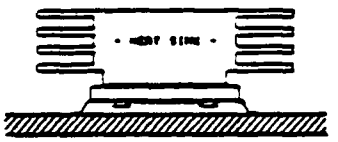
Figure A-22. TriQuint 24/44 Leaded Package; Structure and Specifications

MECHANICAL DIMENSIONS



SUGGESTED MOUNTING

Bending the leads in a gull-wing fashion as shown allows the package to be surface mounted face down. In this way, a heat sink can be mounted on the back of the package, physically close to the die.



PRODUCT DESIGNATIONS

PK-MLC44E	Package body without seal ring, for use with Epoxy seal.
PK-MLC44S	Package body with gold metallized seal ring, for use with AuSn solder lid seal.

Each above product contains: one package body, one lid, and four power supply decoupling capacitors.

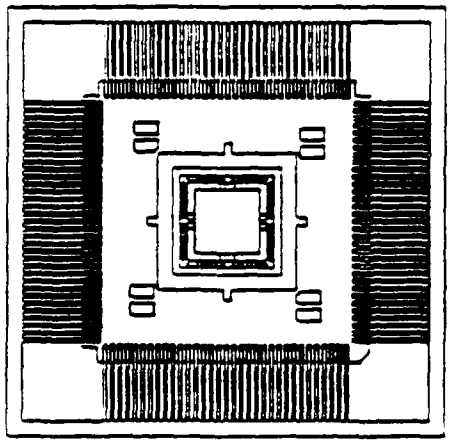
RELATED PRODUCTS

ETF-MLC44	Demountable (solderless) Engineering Test Fixture for the PK-MLC44.

For further information, please contact:

Sales Department
TriQuint Semiconductor, Inc.
Group 700, P.O. Box 4935
Beaverton, OR 97076
(503) 641-4227
FAX: (503) 644-3198

Figure A-23. TriQuint 24/44 Leaded Package; Mechanical Dimensions, Suggested Mounting, Product Designations and Related Products



132 LEAD HIGH SPEED CERAMIC PACKAGE

DESCRIPTION

The MLC132 package is a high-speed multilayer ceramic package developed at TriQuint to support the special requirements of very high performance ICs. The package is designed to handle clock rates up to 3.5GHz and fast edge rates less than 125ps. Signals are carried on 50-Ohm controlled impedance transmission lines from the package leads to the bond pads. Excellent signal isolation is provided by the use of multiple ground lines. Power planes and optional decoupling capacitors minimize switching noise on the power supplies.

The package is fabricated from cofired alumina ceramic. The ceramic package easily handles power dissipation of 1.5 Watts, and can handle 4-5 Watt circuits with the addition of a suitable heat sink. The package is suited for surface mounting with appropriate lead bend. The package body is available with a solder seal ring around the cavity, or without for epoxy sealing.

FEATURES:

- 64 High-Speed 50-Ohm Controlled Impedance Signal Lines
- Power Supply Decoupling via Power Planes and Optional On-Package Capacitors
- Multiple Power and Ground Connections
- Optional Metalized Seal Ring for Hermetic Sealing

April 21, 1988 14-0085-A

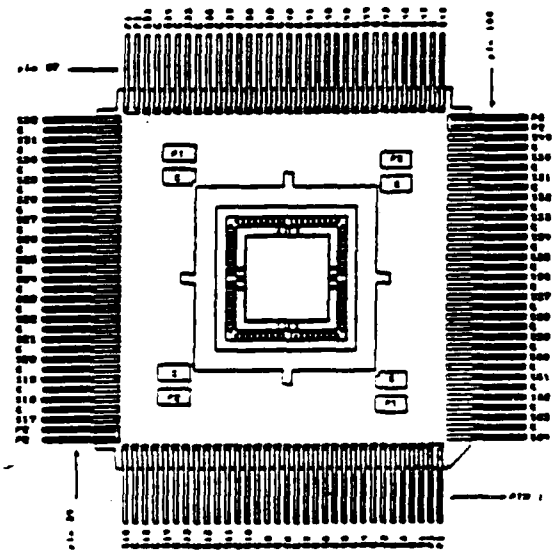
TriQuint SEMICONDUCTOR
A TEKTRONIX COMPANY

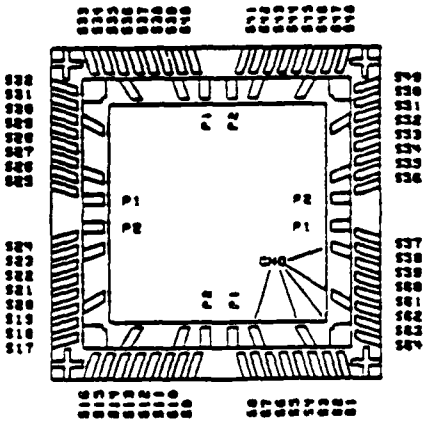
Figure A-24. TriQuint 64/132 Leaded Package; Description

SIGNAL CONNECTIONS

The illustrations below identify package pin and cavity bond pad connections.

Each signal bond pad connects to one package pin through a 50-Ohm controlled impedance line. All the ground bonding pads are connected together, as are all the pins labeled G. All points labeled G or GND are common with all internal ground planes and the back surface of the package. Each of the two power supplies has four pins, two pairs at opposite corners of the package, which are common with four bonding pads, one on each side of the bond cavity. Both power supplies and ground are brought to pads beside the bond cavity where optional decoupling capacitors may be added.



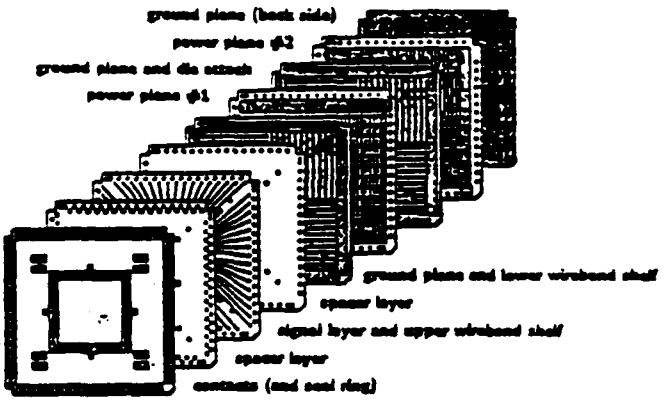


April 21, 1988 14-0085-A

Figure A-25. TriQuint 64/132 Leaded Package; Signal Connections

PACKAGE STRUCTURE

The package is constructed of several metal layers with a layer of ceramic between each pair of metal layers. This structure gives a controlled impedance environment for the signal lines. The figure below shows a representation of the layered structure.



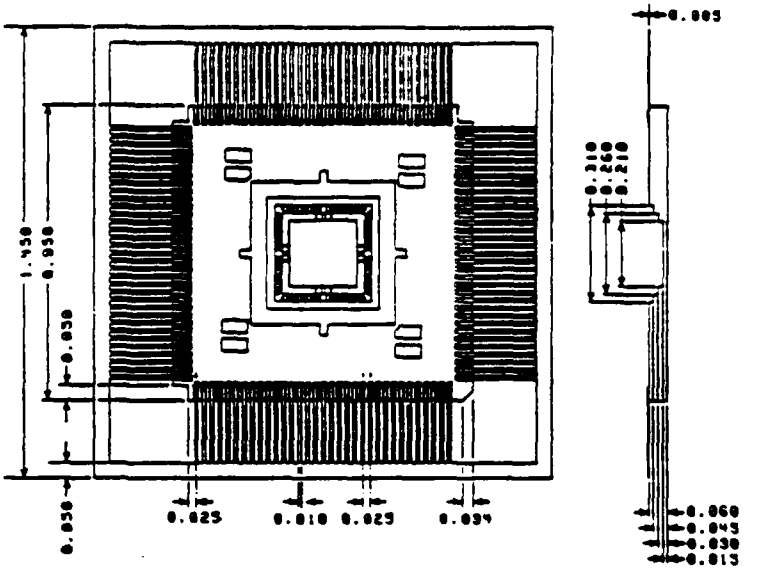
SPECIFICATIONS

Materials:	Body	Alumina Ceramic
	Leads	Kovar
	Metalization	Tungsten/Nickel/Gold
Dimensions:	Body Size	0.950 x 0.950 x 0.080 inches
	Die Cavity Size	0.210 x 0.210 inch
	Max Recommended Die Size	0.170 x 0.170 inch
Leads:	Spacing	0.025 inch
	Lead Count	132
	Signal Leads	64
	Ground Leads	60
	Power Leads	8 (4 per supply)
Misc.	Power Plane Capacitance (each supply)	350 pF
	Pads for Decoupling Capacitor	2/supply
	Recommended Chip Capacitor size	0.050 x 0.080
	Die-to-Case Thermal Impedance[1]	5 °C/Watt

Note [1]: The thermal impedance value shown is typical for a 0.160 x 0.160 die. Use thermal impedance numbers with caution; operating temperature is a complex function of die size, circuit layout, and other factors.

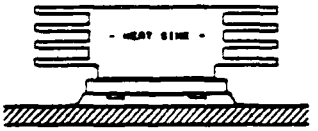
Figure A-26. TriQuint 64/132 Leaded Package; Structure and Specifications

MECHANICAL DIMENSIONS



SUGGESTED MOUNTING

Bending the leads in a gull-wing fashion as shown allows the package to be surface mounted face down. In this way, a heat sink can be mounted on the back of the package, physically close to the die.



PRODUCT DESIGNATIONS

PK-MLC132E Package body without seal ring, for use with Epoxy seal.

PK-MLC132S Package body with gold metalized seal ring, for use with AuSn solder lid seal.

Each above product contains: one package body, one lid, and four power supply decoupling capacitors.

RELATED PRODUCTS

ETF-MLC132 Demountable (solderless) Engineering Test Fixture for the PK-MLC132.

For further information please contact:
Sales Department
TriQuint Semiconductor, Inc.
Group 700, P.O. Box 4935
Beaverton, OR 97076
(503) 641-4227
FAX: (503) 644-3198

Figure A-27. TriQuint 64/132 Leaded Package; Mechanical Dimensions, Suggested Mounting, Product Designations and Related Products

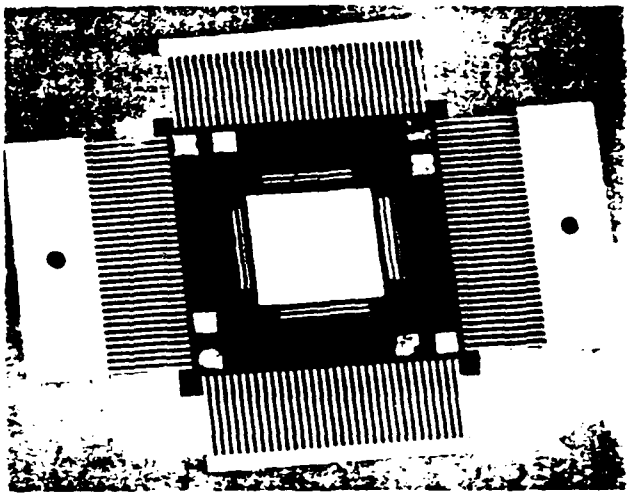
Bulletin 103

Leaded Polyimide Chip Carriers

High Performance Series (PHIP)
High I/O Count Series (PHIL)

Features

- **Microstrip Construction**
  ... for High Performance Circuit Applications
- **High Interconnect Densities** with 132 and 164 Leads
- **IC Bonding Pads on 0.010" Centers and I/O Leads on 0.025" Centers**
  ... to Facilitate Interconnections
- **Controlled Impedance (PHIP Only)**
  ... 50 Ohm Standard, 25 to 75 Ohm Available; for low transmission and return loss and high system performance
- **Integral Heat Sink**
  ... Die Bonded Directly to Heat Sink for Cooler Operation and Higher Reliability
- **Provisions for Four Capacitors Directly on the Chip Carrier**
  ... for Improved Decoupling



Augat Microtec offers high performance chip carriers (PHIP Series), employing the unique Copper-Polyimide "additive" process ideally suited to applications involving CMOS, ECL, GaAs and other semiconductor technologies which require high density interconnect, thermal management and controlled impedance characteristics. These carriers provide high performance and improved environmental protection, and feature superior electrical characteristics, as well as JEDEC conformance.

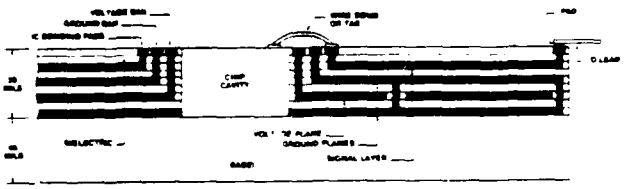
Also available is a companion series (PHIL) of chip carriers, for applications requiring only high I/O densities. These more economical units differ from the high performance (PHIP) series in that ground planes, controlled impedance signal lines, and provisions for integral capacitors have been deleted.

Augat Microtec Polyimide Chip Carriers utilize the firm's "additive" process, which facilitates customization to fit virtually any special high speed application. A wide range of signal, power and ground layers, with appropriate via layers, may be designed into the chip carrier.

Performance Specifications

Dielectric Constant	3.8
Capacitance	<1 pf
Resistance	<30 mΩ
Inductance	<2 nh

MICROSTRIP CONSTRUCTION



To Order, specify...

PHIP Part No.	PHIL Part No.	Leads	I/O	O.D	Cavity	Z_0 (Ω)	Gnd	Co-Planar	Base** Material
P132-001		132	.025	.950" x .950"	.400	50	Yes	Yes	Copper
	L132-001	132	.025	.950" x .950"	.400	N/A	N/A	N/A	Copper
P164-001		164	.025	1.150" x 1.150"	.400	50	Yes	Yes	Copper
	L164-001	164	.025	1.150" x 1.150"	.400	N/A	N/A	N/A	Copper

Notes: ** **Optional Base Materials**
- BEO
- Aluminum
- Copper/Invar/Copper

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11/86

Figure A-28. Rogers 116/132 and 148/164; Features and Specifications

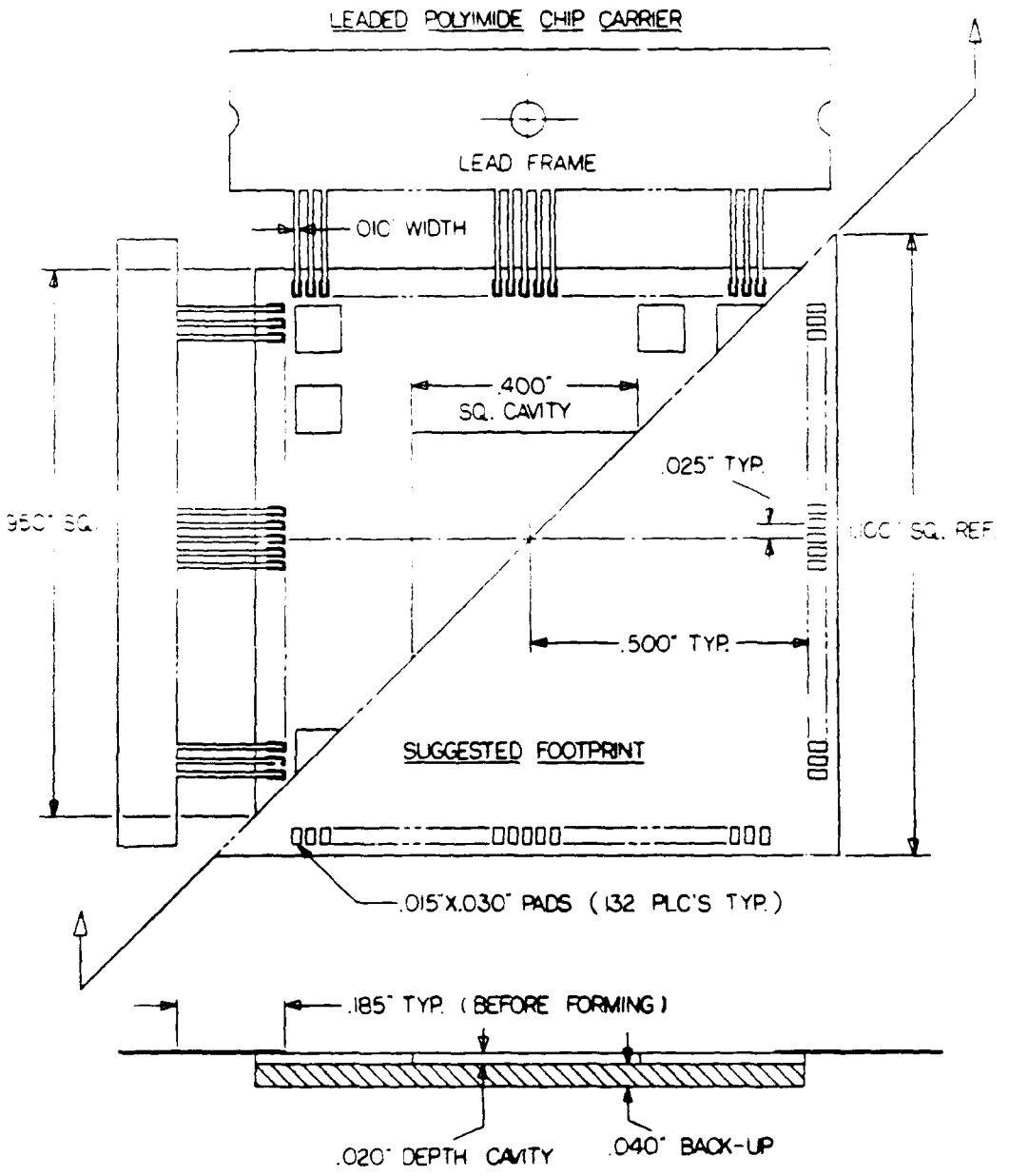

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Figure A-29. Rogers 116/132 Leaded Package, P-132-001; Mechanical Dimensions

WIRING DIAGRAM
FOR
P132-001

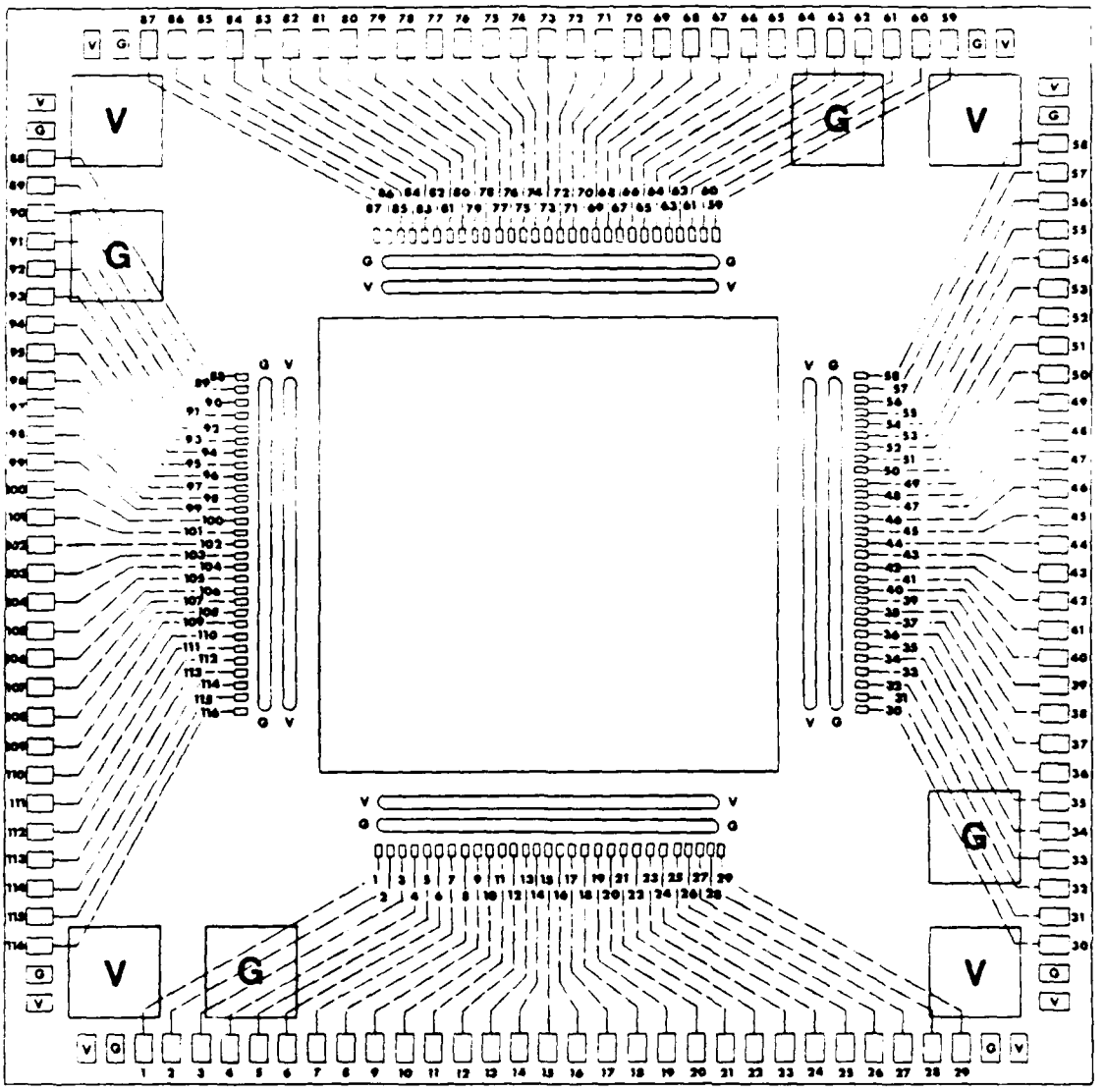

Figure A-30. Rogers 116/132 Leaded Package, P-132-001; Wiring Diagram

AUGAT MICROTEC

P164-001

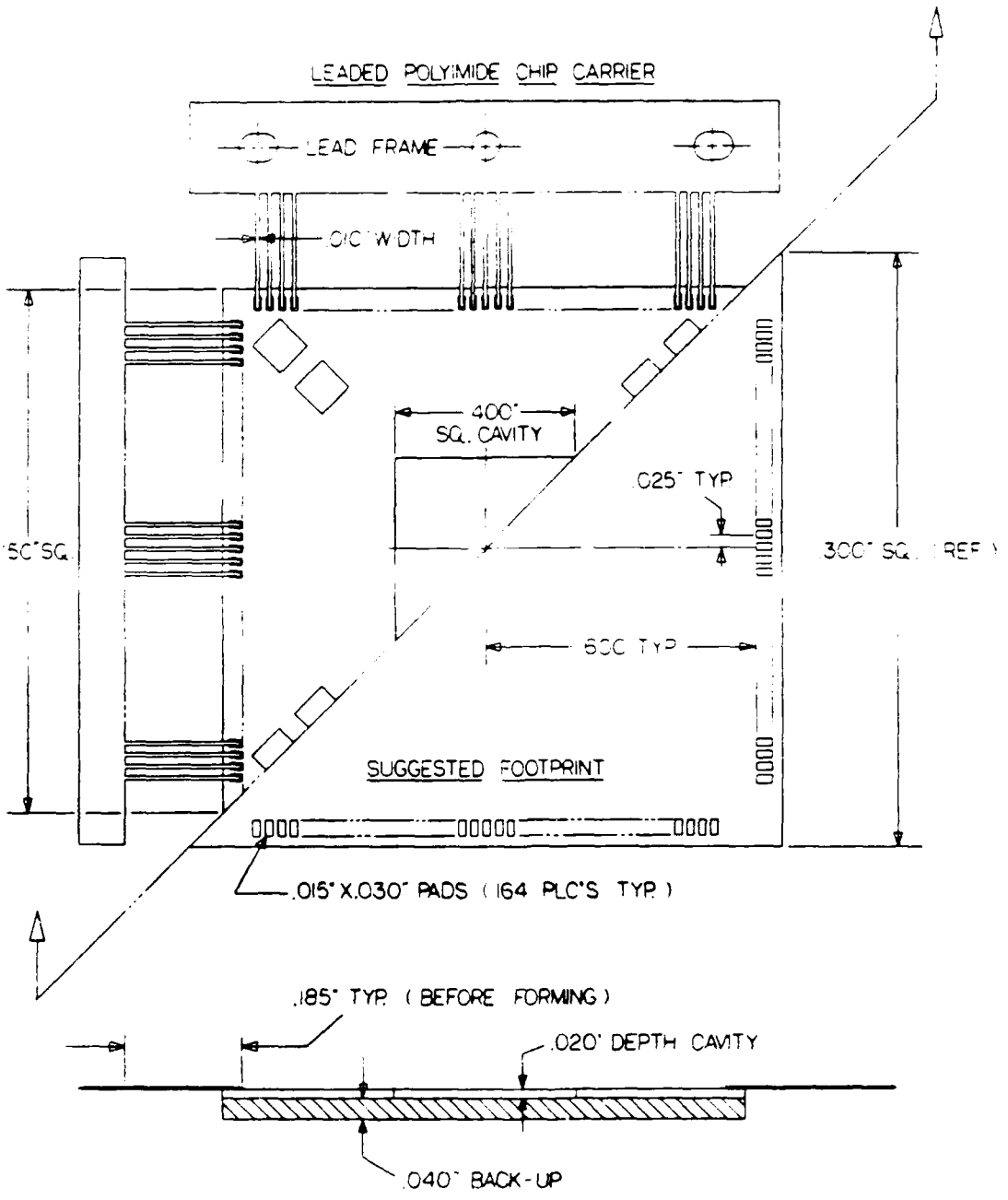

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Figure A-31. Rogers 148/164 Leaded Package, P-164-001; Mechanical Dimensions

WIRING DIAGRAM
FOR
P164-001

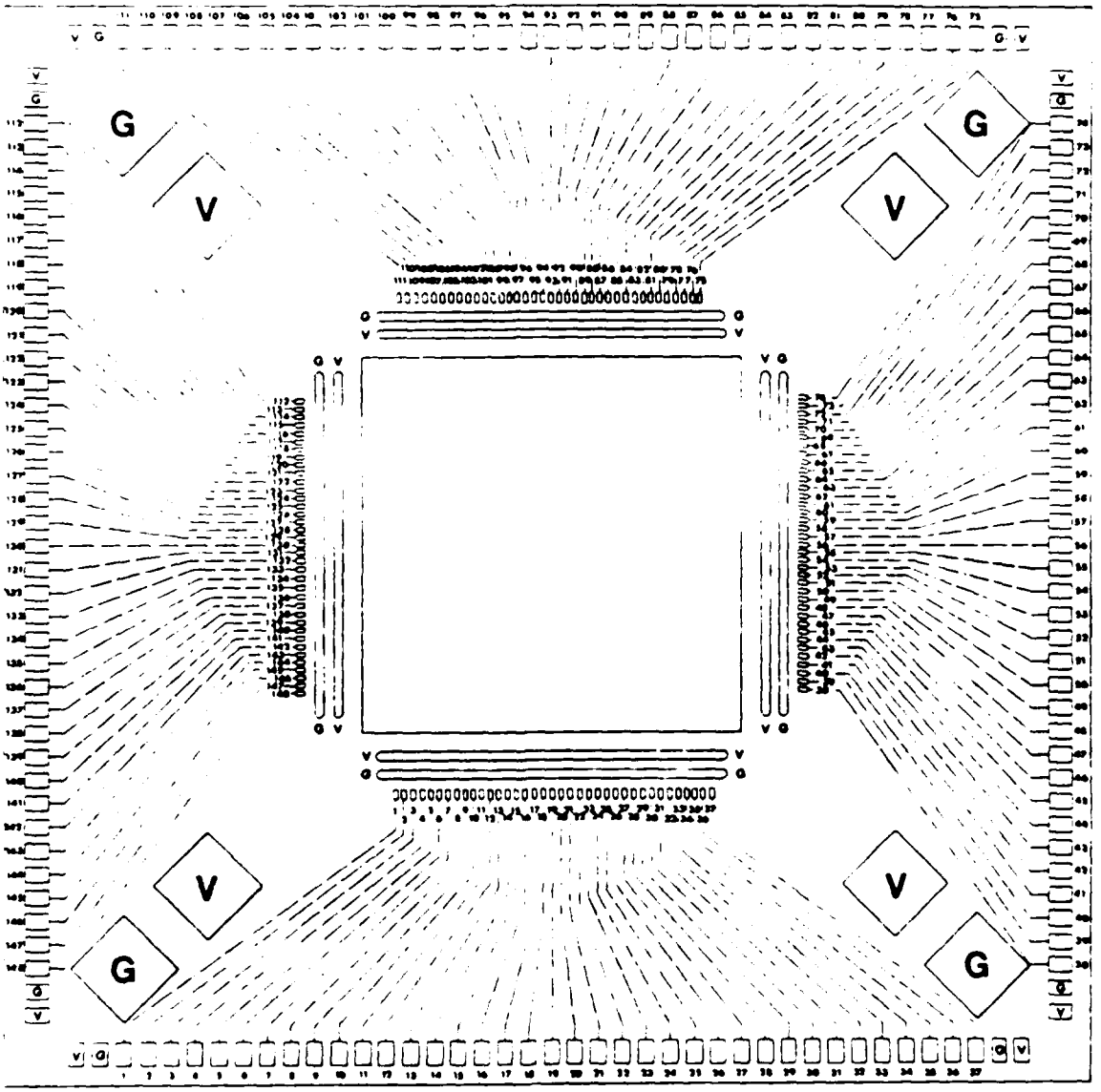
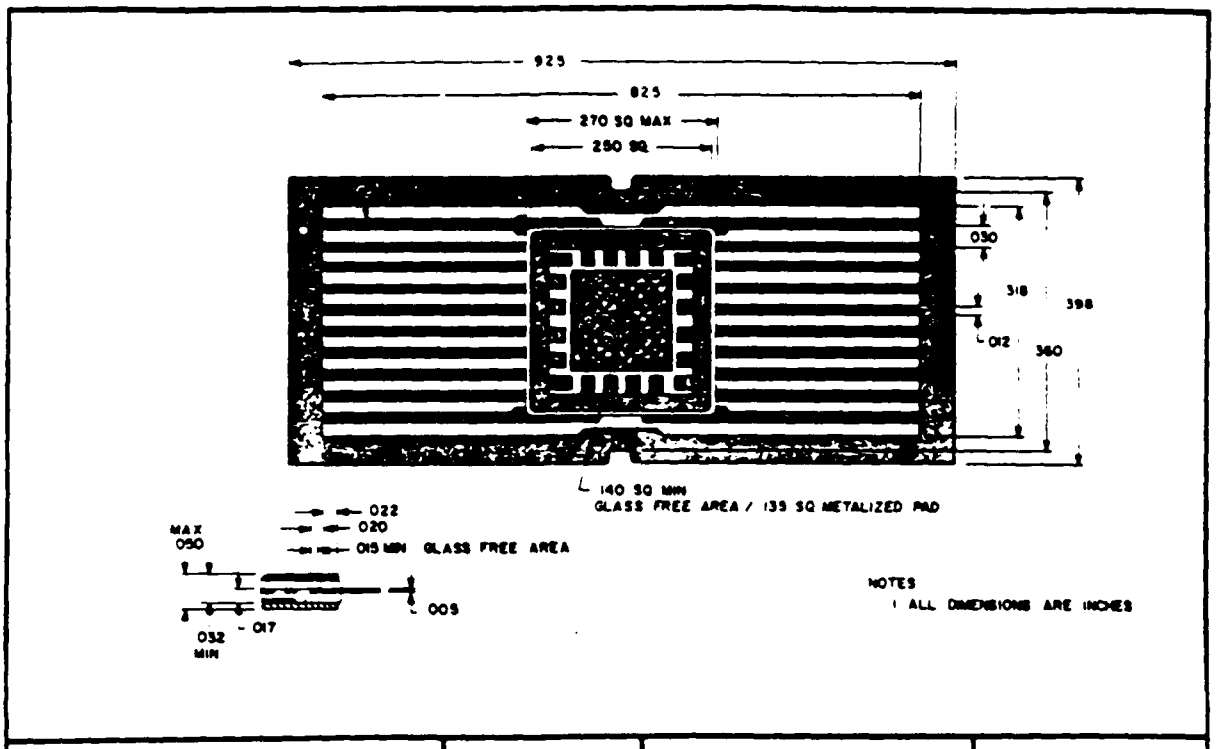


Figure A-32. Rogers 148/164 Leaded Package, P-164-001; Wiring Diagram

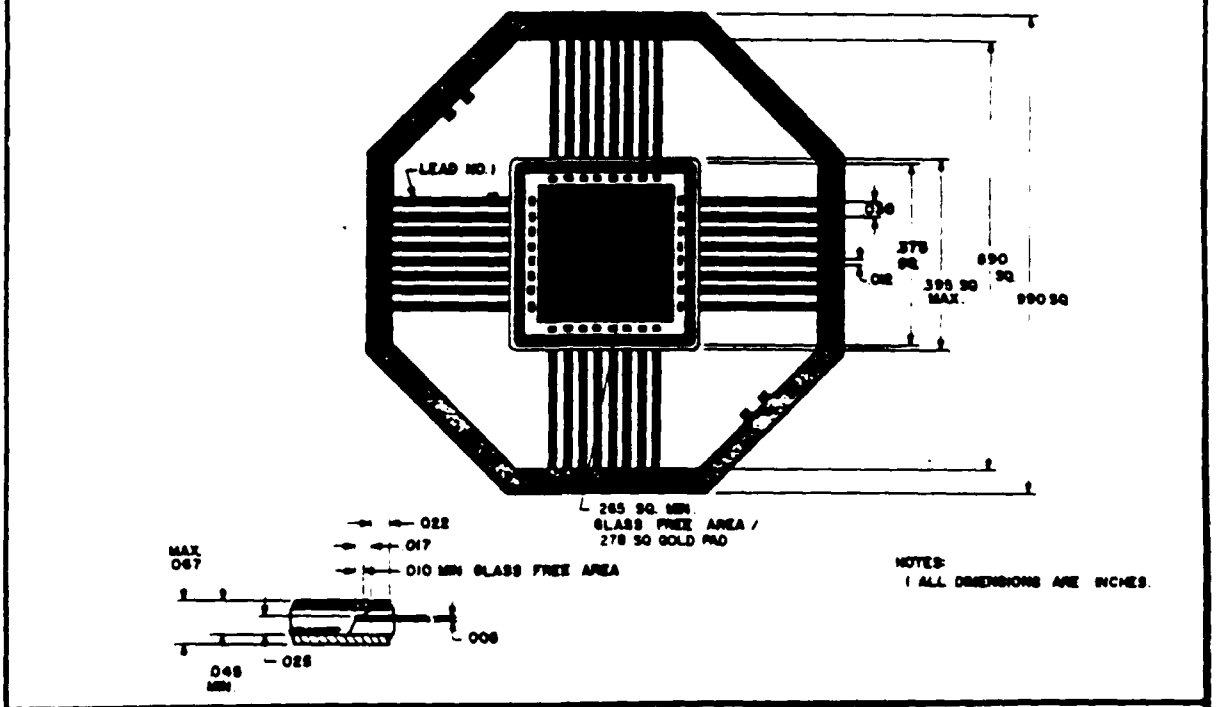
ELECTRONIC PACKAGE DIVISION
58 EAST BACON ST P O BOX 1397
PLAINVILLE MA 02762

MINI-SYSTEMS, INC.

(617) 695-2000
TWX (710) 348-0564



METALIZED CERAMIC BASE	20 LEADS	.140 x .140	3H20CM



METALIZED CERAMIC BASE	32 LEADS	.265 x .265	3LN32CM

Figure A-33. MSI 20/20 (Upper), MSI 32/32 (Lower)

ELECTRONIC PACKAGE DIVISION
168 EAST BACON ST. P.O. BOX 597
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MINI-SYSTEMS, INC

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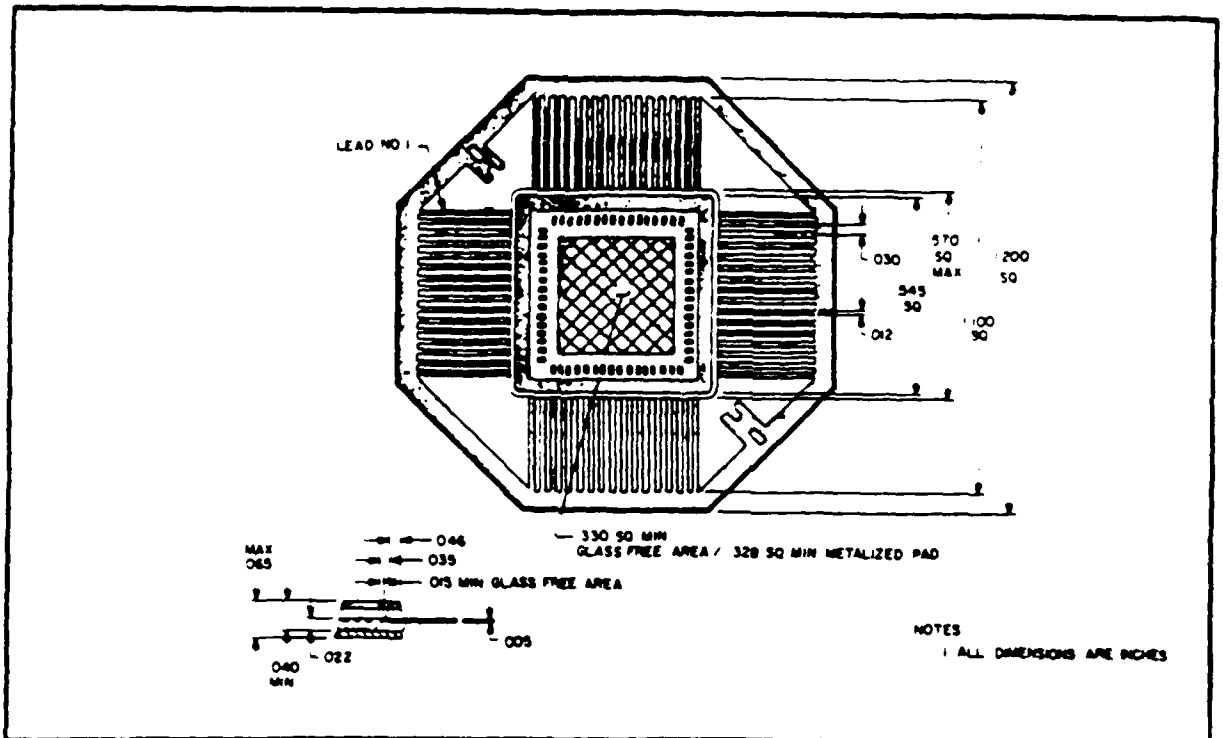
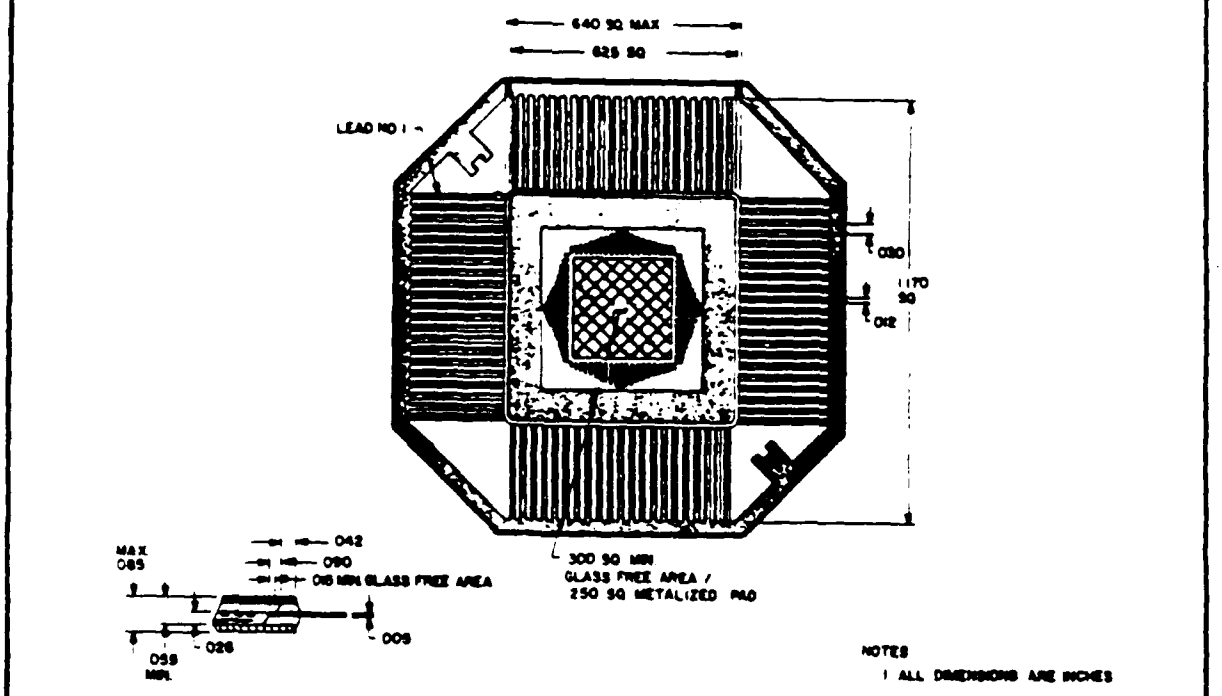
TWX (710) 348-0564



METALIZED CERAMIC BASE	64 LEADS	.330 x .330	3T64CM



METALIZED CERAMIC BASE	84 LEADS	.300 x .300	3U84CM

Feb 1983

Figure A-34. MSI 64/64 (Upper): MSI 84/84 (Lower)

Drawings for Packages

Described in Table A-2

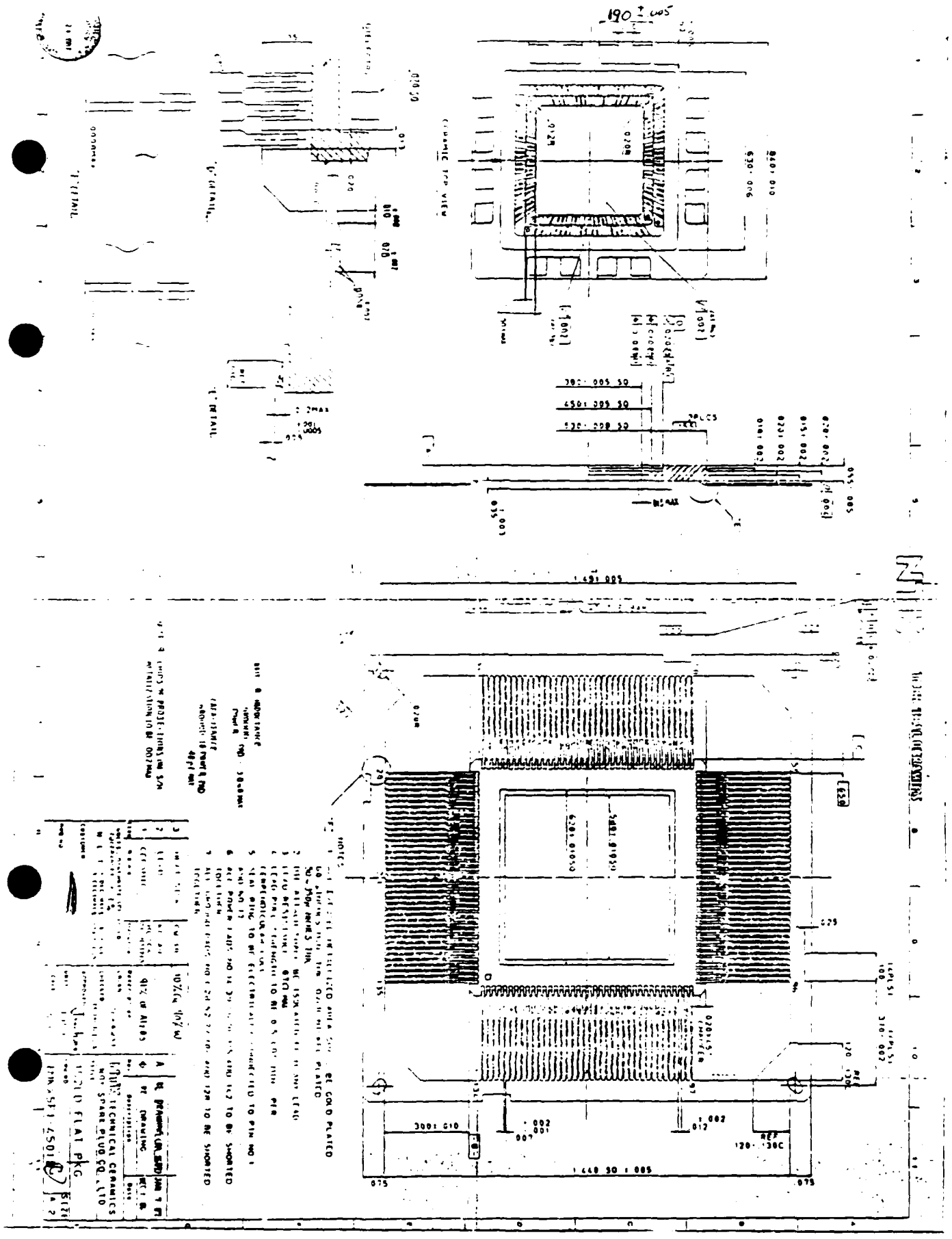


Figure A-35. NTK 152 Leaded Package

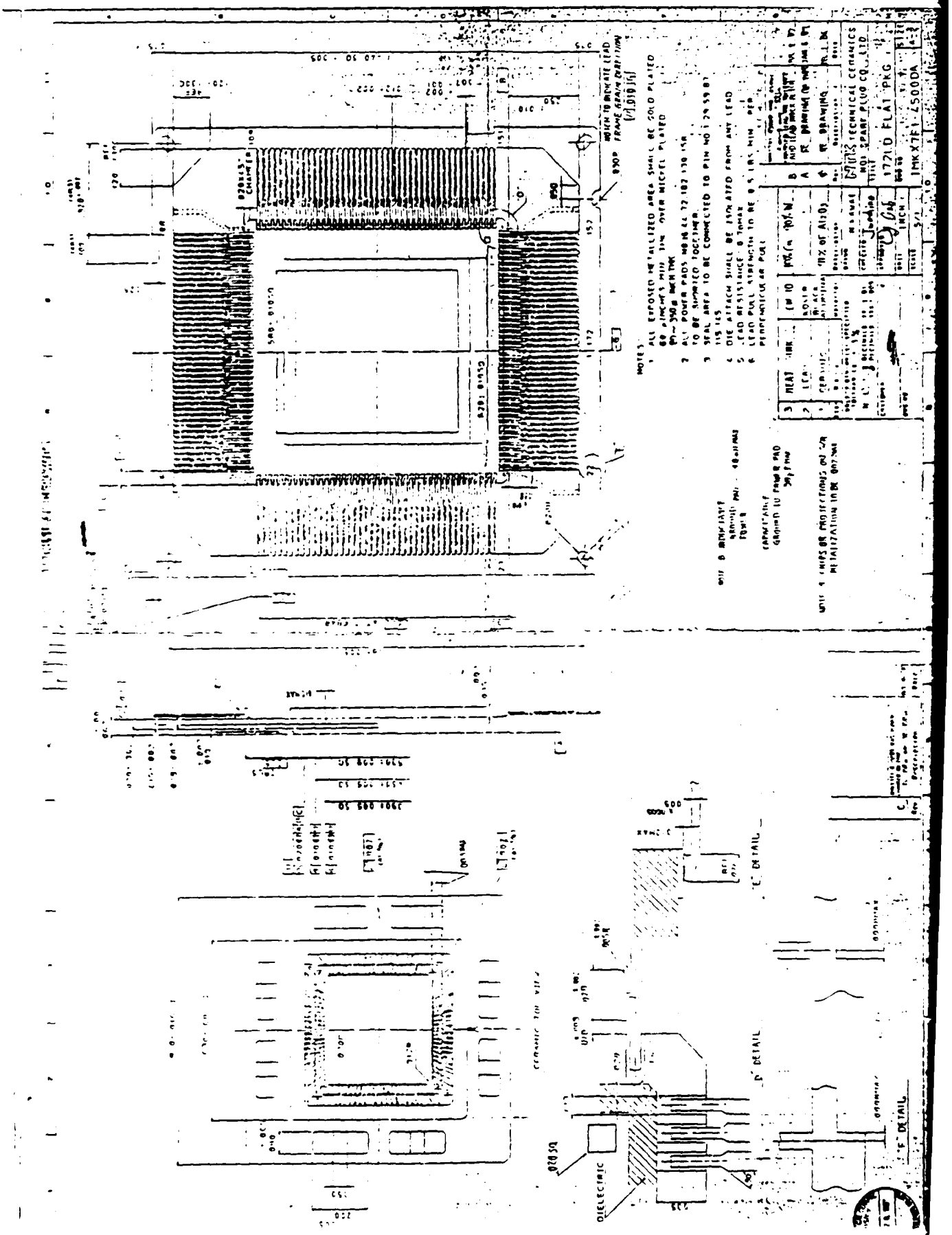


Figure A-36. NTK 172 Leaded Package

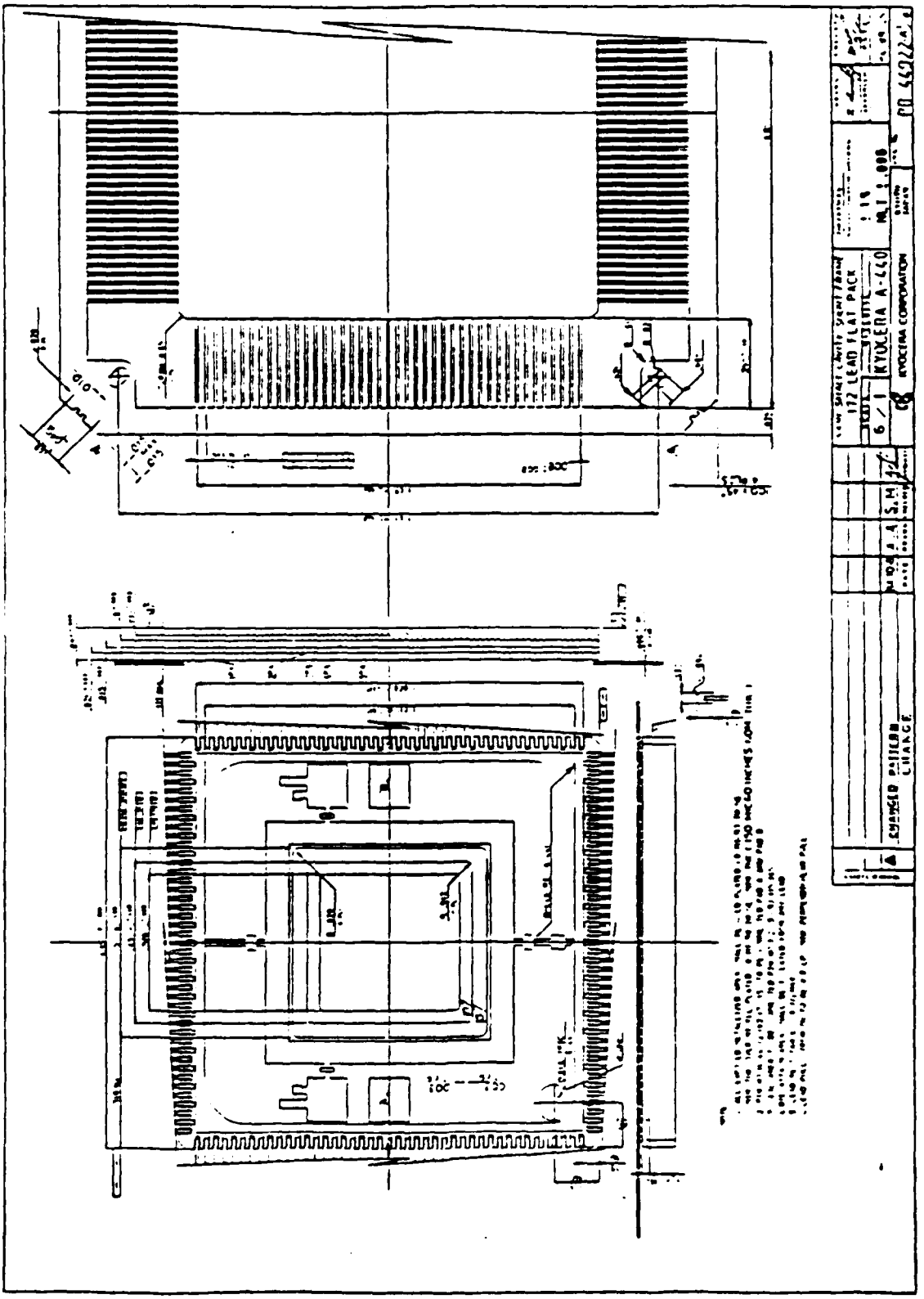


Figure A-37. Kyocera 172 Leaded Package

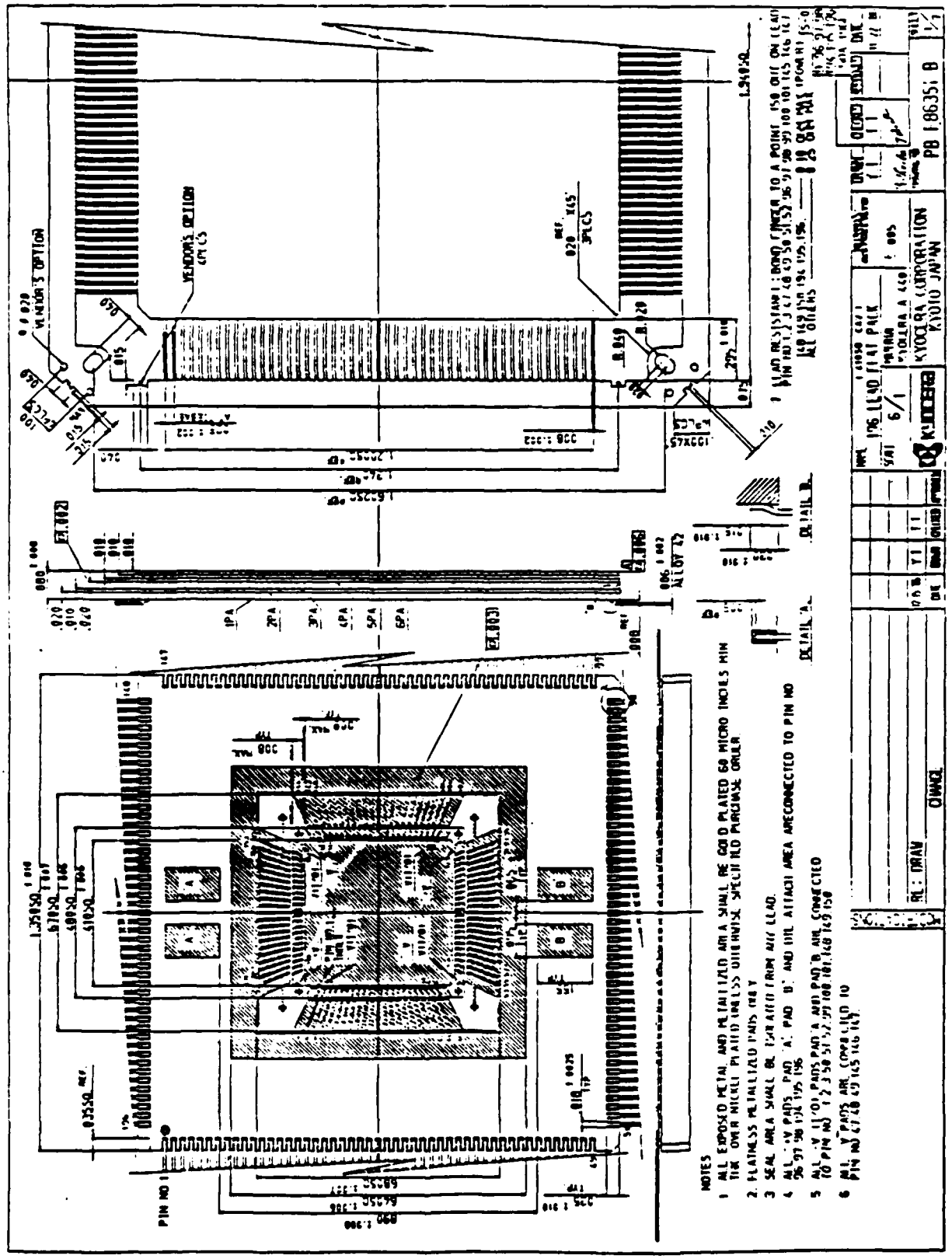


Figure A-38. Kyocera 196 Leaded Package

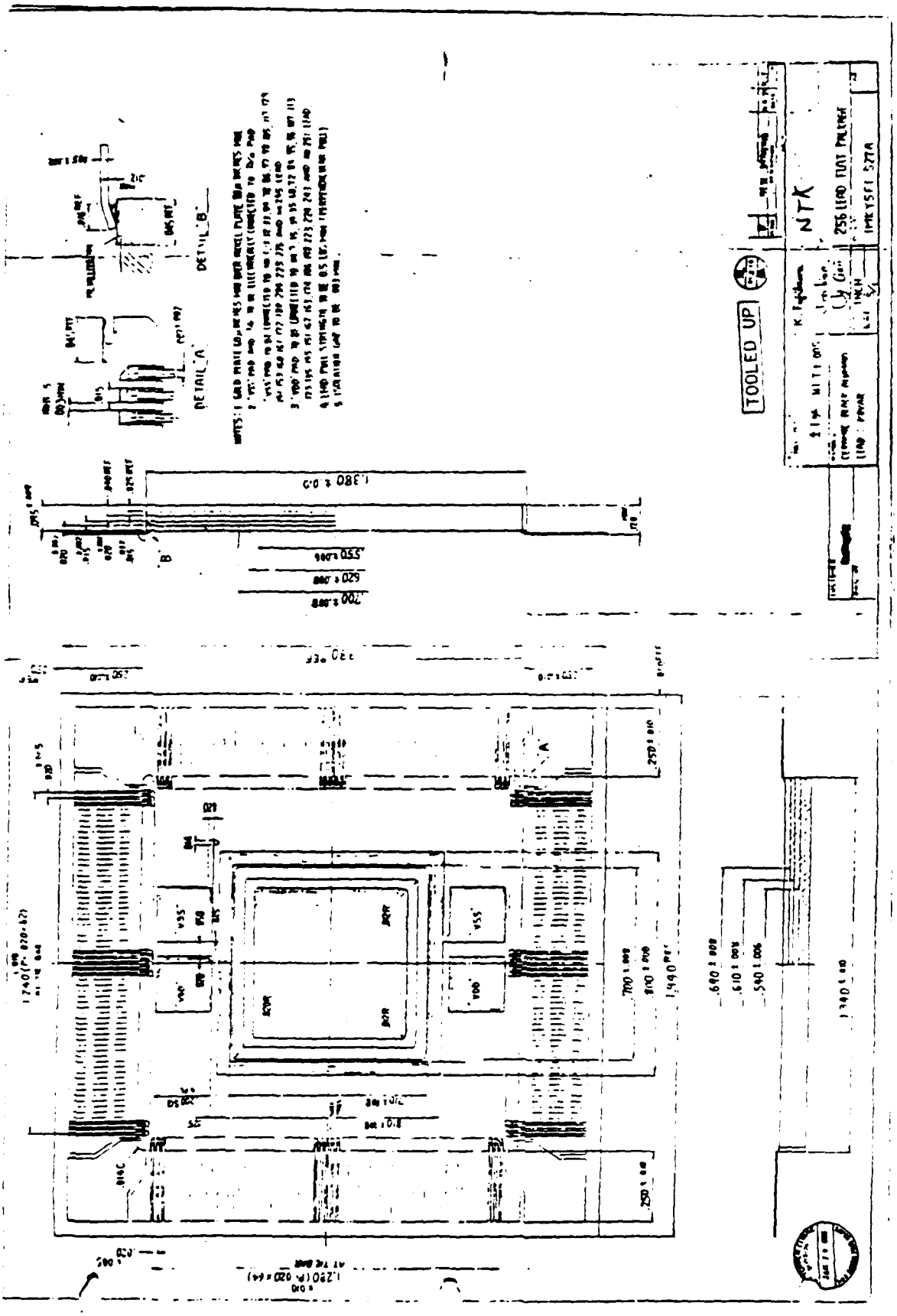


Figure A-39. NTK 256 Leaded Package

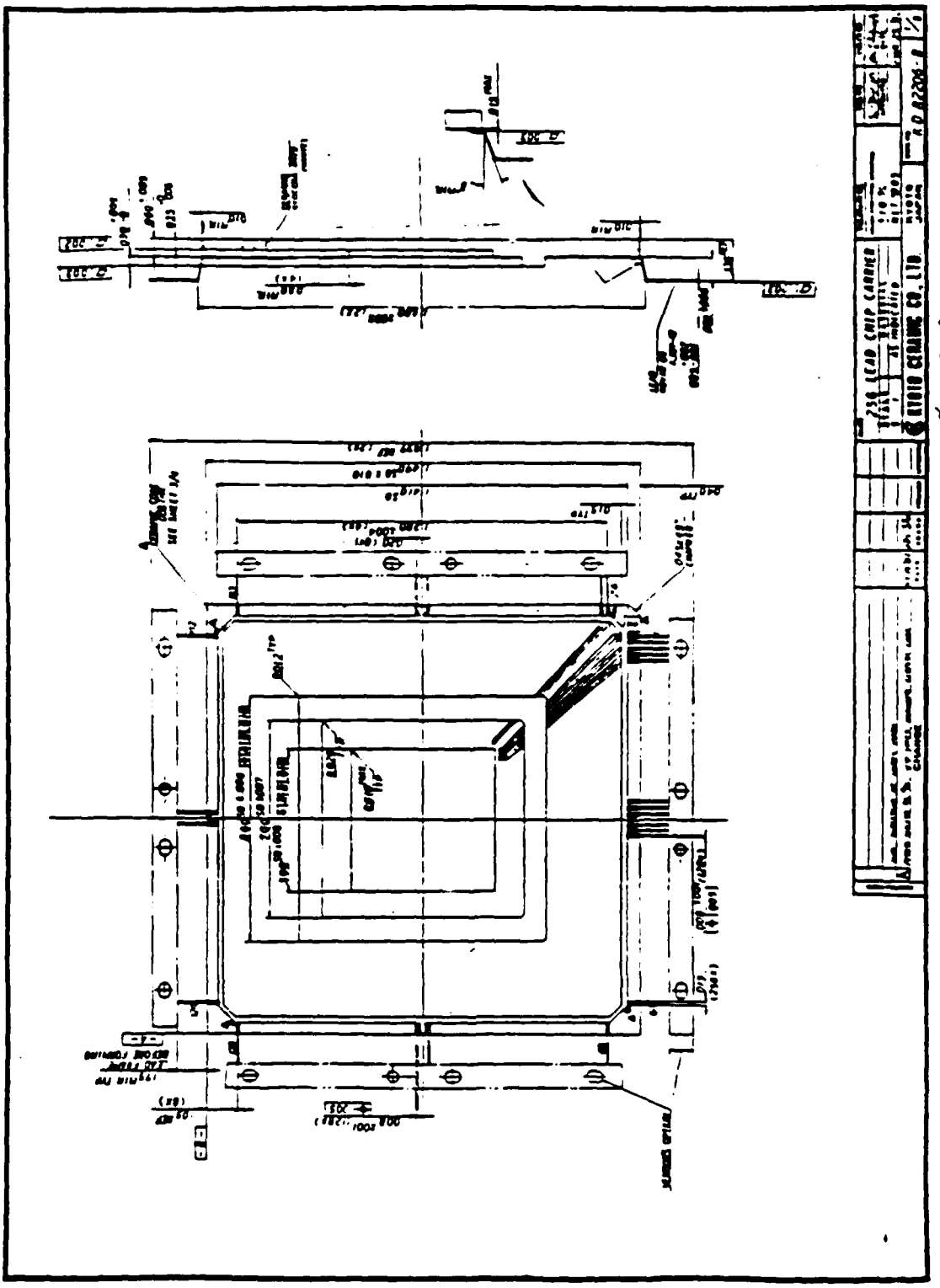


Figure A-40. Kyocera 256 Leaded Package

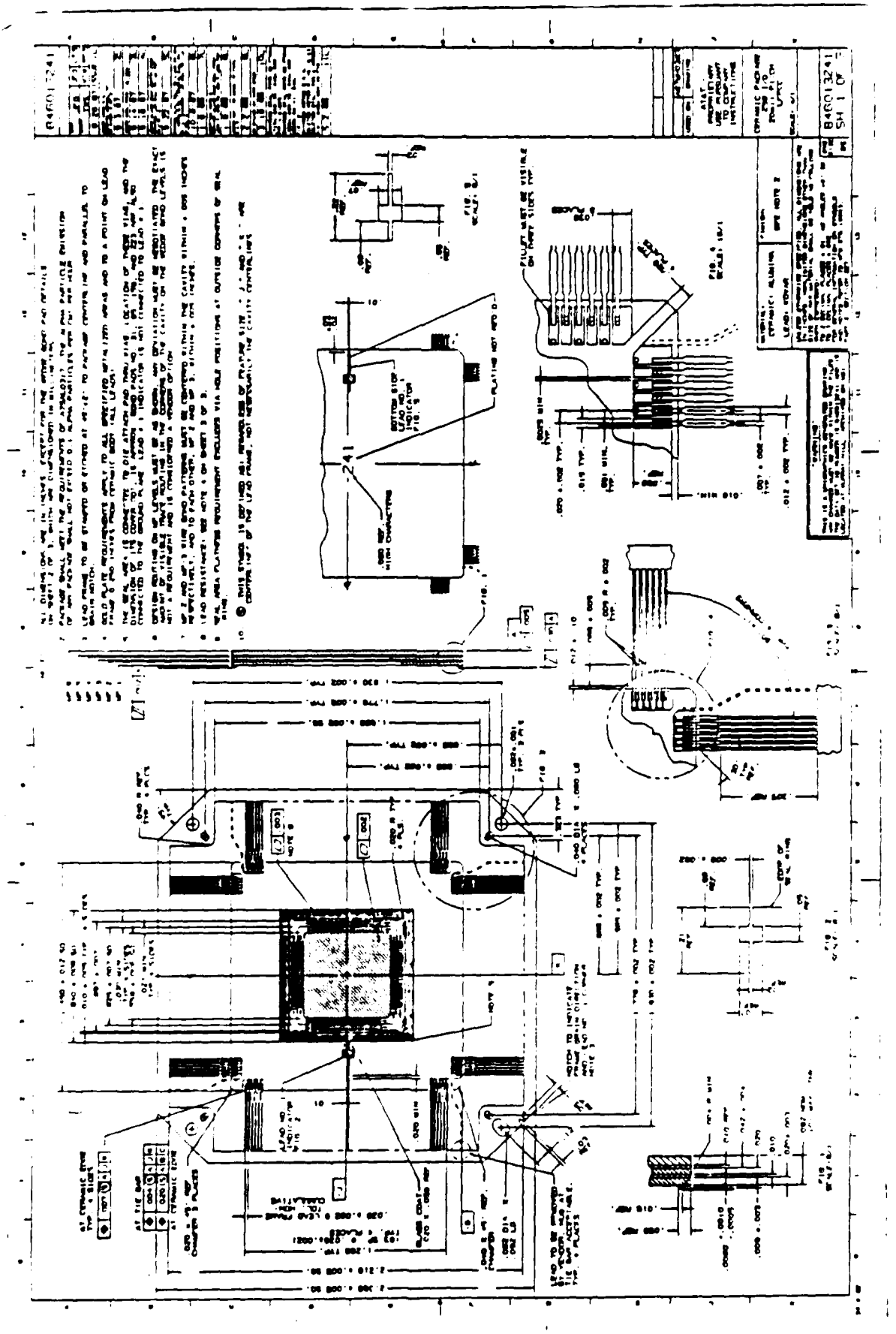


Figure A-41. NTK 256 Leaded Package: AT&T Design, Mechanical Dimensions

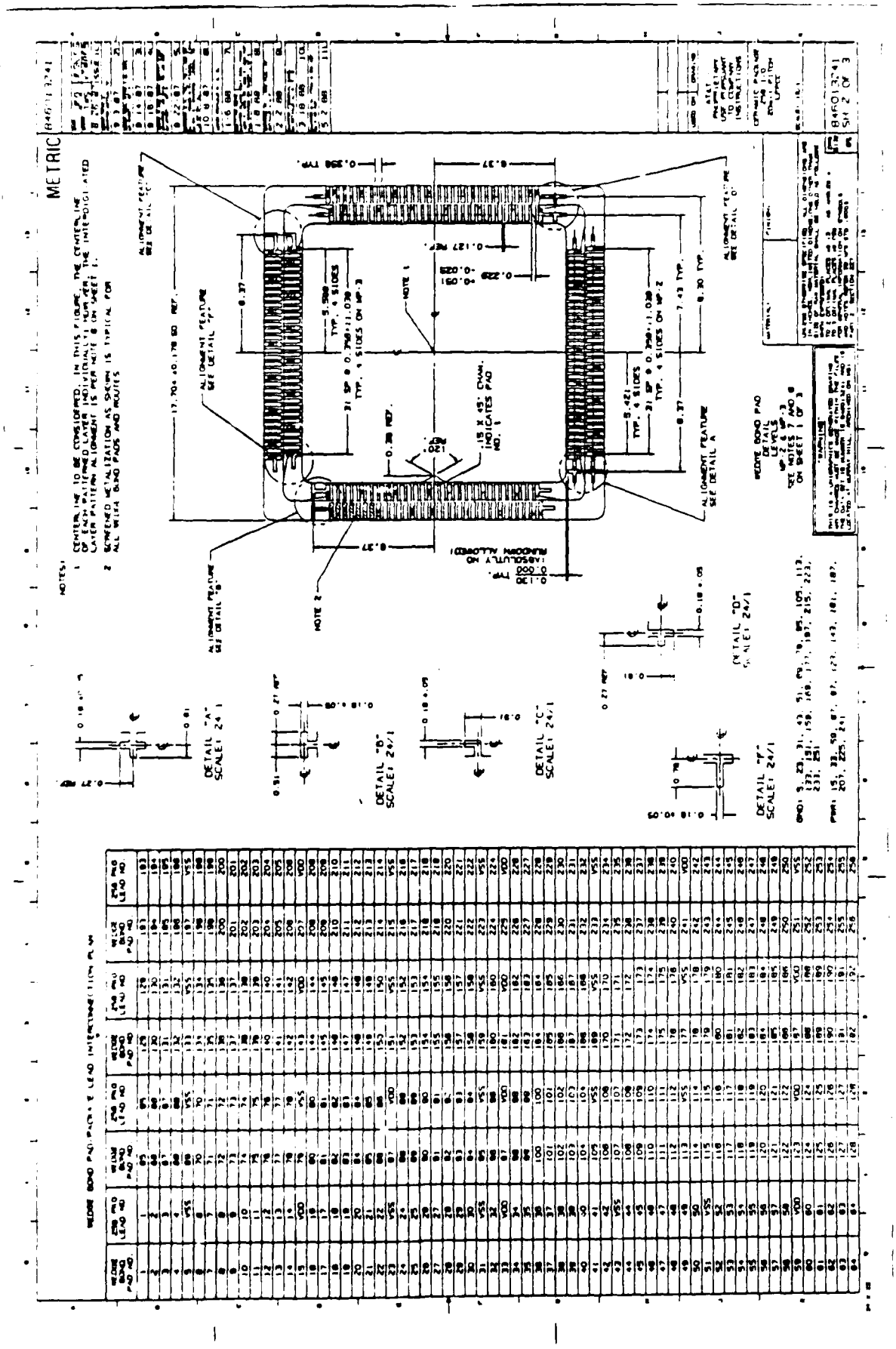


Figure A-42. NTK 256 Leaded Package; AT&T Design, Pin Assignment

APPENDIX B

Reliability Plan for the DARPA III Pilot Line Program

(Y. L. Cho and R. L. Remke)

RELIABILITY PLAN FOR THE DARPA III PILOT LINE PROGRAM *

Y. L Cho and R. L. Remke
AT&T Bell Laboratories
Reading, PA 19612
June 14, 1988

1. INTRODUCTION

The major purpose of the reliability evaluation procedure is to determine the median life time[1] (MLT) of the GaAs circuits fabricated on the DARPA III Pilot Line. In this reliability procedure, one circuit from each family of circuits (logic and memory) will be subjected to high temperature operating bias (HTOB) aging at three different temperatures. Testing will allow the determination of the failure distribution, failure mode activation energy, and MLT. The reliability tests will follow the general guidelines of MIL-STD-883C, Method 1016, where appropriate. In addition, the reliability evaluation module (REM) will be used to evaluate circuit elements and structures, and identify potential reliability problem areas. The results from all the reliability tests will be fed back to the design, materials, and processing areas so that corrective action can be taken, if necessary.

2. RELIABILITY TEST CONSIDERATIONS

2.1 Selection of Devices

Since all the device codes (both logic, and memory) are based on the same SARGIC (Self Aligned Refractory Gate Integrated Circuit) technology and metallization system, one representative device code from each family (logic and memory) will be tested. This grouping of codes into families follows the same procedures used in our internal AT&T GaAs and silicon reliability studies and provides the greatest statistical confidence level for the amount of devices tested. The logic and memory reliability test vehicles will be the ALU (Custom A) and the 4K SRAM, respectively. The ALU is one of the first circuits fabricated and will provide the first reliability data. The results of FMA on ALU failures will be fed back into circuit design, materials, and processing for corrective action (if necessary). Since SRAMs are often used as benchmarks for speed, complexity, etc, the reliability evaluation of the 4K SRAM will provide data for comparison with other GaAs and silicon technologies. The reliability testing will use 250 units each of the ALU and the 4K SRAM devices.

2.2 Burn-in/prescreen

Semiconductor devices (with no burn-in or prescreening) that are subjected to normal or above normal operating stress usually follow a particular failure distribution pattern. In general, there

---

* Note: Since the inital submission of this plan on June 14, 1988, the PT-2M has been substituted for the ALU as the first reliability evaluation circuit. This change was primarily made so that reliability testing could begin earlier.

will be a cluster of early failures (infant mortality), usually followed by failure mechanisms that take longer to occur. For integrated circuit production, the infant mortality failures are removed before shipment by a burn-in procedure. For this program, a burn-in operation will not be performed on some of the samples so that the infant mortality may be evaluated and an appropriate burn-in procedure developed. The initial burn-in operation will be the one we use on our GaAs lightwave codes (125°C for 20 hours).

2.3 Reliability Testing

The reliability of the devices can be estimated from accelerated life tests that induce failures within a reasonable time period. The proposed plan uses the HTOB test as the reliability/life characterization tool. The HTOB apparatus and aging/test procedure are described below.

A. Apparatus

1. Device sockets and aging fixtures: Suitable high temperature sockets and aging fixtures will be used for electrical contacts.
2. Heat chamber: The aging fixture will be placed in a forced air convection chamber. The chamber will be equipped with appropriate over temperature protection and external temperature recording device.
3. Bias and monitoring circuits: The DC bias and monitoring system will be capable of supplying the specified bias, and sensing device voltages and currents.

B. Aging/Test Procedure

1. Test conditions: Three different ambient aging temperatures (150, 175, and 200°C) will be used in the HTOB experiments for determining the activation energy. These ambient temperatures were chosen because previous reliability aging of GaAs FETs showed a change in the failure activation energy above 200°C. The channel temperatures will be measured using liquid crystals or infrared measurements. The circuits will be DC biased with inputs and outputs appropriately terminated. The test conditions, device serial number, and device position in the fixture will be recorded.
2. Measurements and duration of the aging: All the electrical measurements will be made as soon as possible after removal of the device from the aging conditions. The planned measurement points will be at 0, 100 300, 600, and 1000 hours for 175 and 200°C aging. Aging will continue up to 3000 hours for the 150°C test, when necessary.
3. Aging system verification: The aging setup will be verified initially, and monitored periodically thereafter. Device sockets and connectors to the aging fixtures will be checked to verify electrical continuity.
4. Failure definition: A failure will be defined as a specified percentage change in any of the critical circuit parameters. The percentage change will be based on expected system requirement tolerances (typically, 10 to 20%).

2.4 Statistical Modeling

The reliability testing will allow the determination of the failure distribution, failure mode activation energy, and MLT (including the confidence limits). To show the statistical modeling to be used in calculating the above parameters, an example is described below using previous data on GaAs pre-amp circuits.[2]

The failure distribution can be determined by analyzing the time to failure for the circuits under test. In Figure B-1, the time to failure data for the GaAs pre-amp circuits is plotted. On the lognormal probability paper used for the plot, the straight line obtained for each of the three test temperatures shows that the failure distribution mechanism of the GaAs circuits follows a lognormal failure distribution. The lognormal failure distribution has been consistently observed for GaAs and silicon devices. However, determination of the failure distribution from the data is not always as straightforward. If more than one failure mechanism is involved, the distribution for each mechanism must be determined.

The failure rate of GaAs circuits can be accelerated by increasing the temperature of the circuits during the test. This acceleration factor A can usually be described by the Arrhenius relationship,

$$A = \frac{\tau}{\tau_o} = \exp\left[\frac{E_a}{k}\left[\frac{1}{T} - \frac{1}{T_o}\right]\right]$$

where τ is the MLT at the desired temperature (T) in °K, τ_o is the MLT at the aging temperature (T_o) in °K, E_a is the activation energy, and k is the Boltzmann constant. Testing at different temperatures enables one to calculate the activation energy, and therefore the MLT at any use temperature. Figure B-2 shows a graphical technique for finding MLT at any use temperature. In addition, the failure rate at typical use conditions will be determined from the failure distribution and the MLT.

2.5 FMA

The failed circuits from the reliability experiments will be analyzed using our GaAs FMA techniques. The FMA goal will be to identify the locations and physical reasons for the failures and feed the information back into the design, materials, and processing for corrective action. Typically, the failed circuits will be electrically analyzed, looking for clues to the failure. The package will then be opened and visually examined. Photographs will be taken of the circuits, and compared to the pretest photographs. Further analysis such as electron beam probing or electro-optic probing may be used to identify the location of the failure. Other FMA techniques such as SEMs with and without voltage contrast, EBIC (electron beam induced current), XPS (x-ray photoelectron spectroscopy), AES (Auger electron spectroscopy), and SIMS (Secondary ion mass spectrometry) will be used as necessary.

2.6 Reliability Evaluation Module (REM)

The REM includes capacitors, crossovers, and electromigration testers. Early electromigration studies are now in progress, and results from these tests and upcoming tests on the above components will be fed back into the design, materials, and processing areas for corrective action if necessary.

3. RELIABILITY PLAN SCHEDULE

Table B-1 shows a time schedule for the reliability plan. Tests are in progress and will continue using the REM, followed by reliability tests on the ALU and the 4K SRAM, respectively.

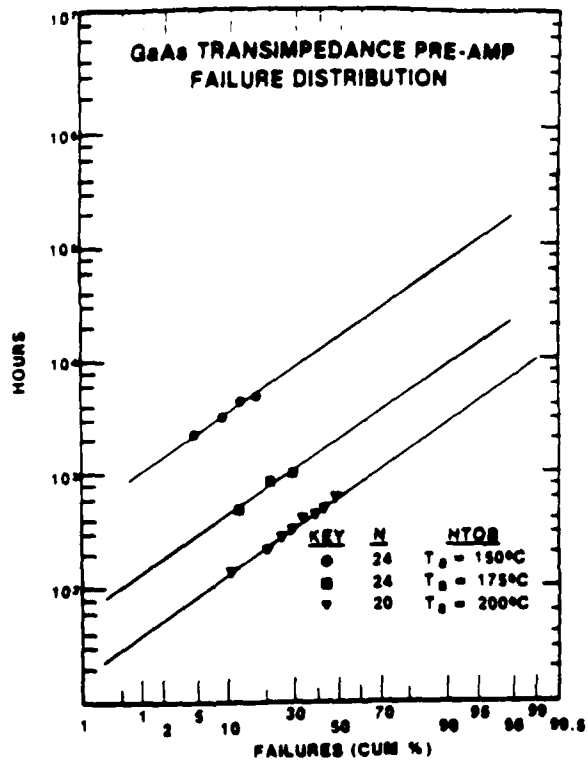


Figure B-1. The failure distribution for three HTOB aging conditions plotted on lognormal probability paper.

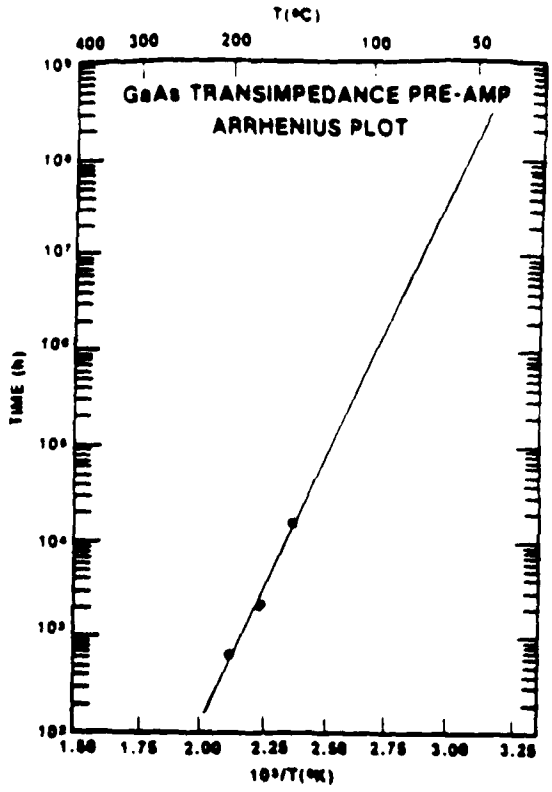
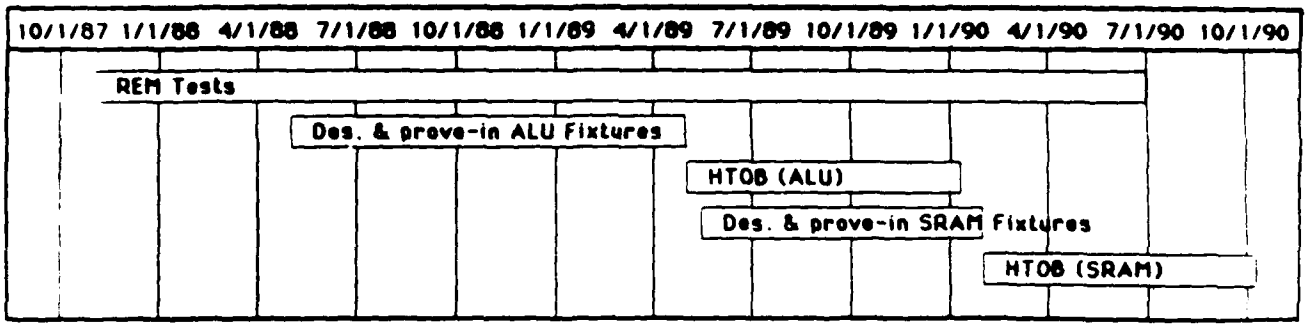


Figure B-2. Arrhenius plot of the three MLT values obtained from Figure B-1. The curve is projected to obtain expected MLT values at lower aging temperatures.

Table B-1 - Reliability Plan Schedule



REFERENCES

1. MIL-STD-883C, Method 1016

2. M. Spector and G. A. Dodson, "Reliability Evaluation of a GaAs IC Pre-amplifier HIC," GaAs IC Symposium, October 1987.